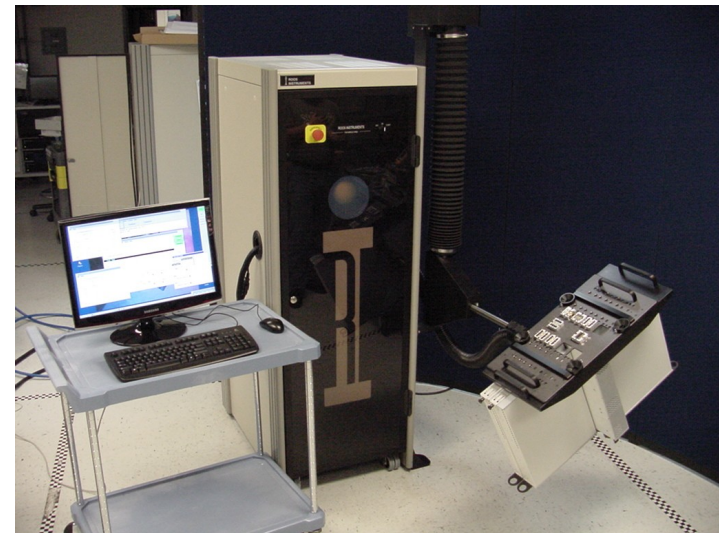




CASSINI RF/ Microwave ATE System Application Development by Example



ROOS INSTRUMENTS



LNA Tests

- DC Currents & Beta
- S11, S21, S12 & S22
- Noise Figure
- P1dB
- Intermodulation Distortion
- Harmonics



Search Measurements

- Dependent and Independent Variable
- Collect appropriate data
- Curve fit
- Find desired dependent condition
- Retrieve associated independent stimulus



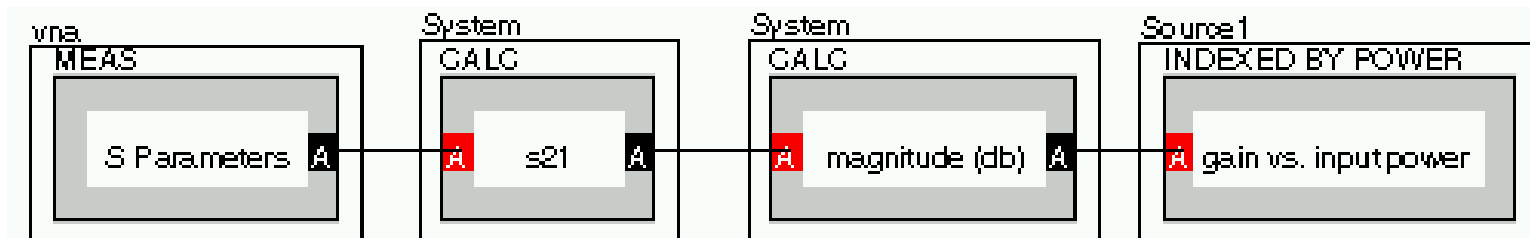
P1dB, Step 1 and 2

- Measure the small signal gain, in this case 10 dB
- Subtract 1 from the value to establish the "target compression gain" in this case 9 dB



P1dB Step 3

- Measure gain at a number of Source 1 input power levels, saving the measured gains, indexed by Source 1 Power.





P1dB Step 3 (Continued)

- The index value is actually not the Source 1 power value, It is the "N" as in the Nth value of the Source 1 power used

<i>Index, Gain</i>	
1,	10
2,	10
3,	10
4,	10
5,	10
6,	9.7
7,	9.2
8,	8.4
9,	7.5
10,	6.5
11,	5.5

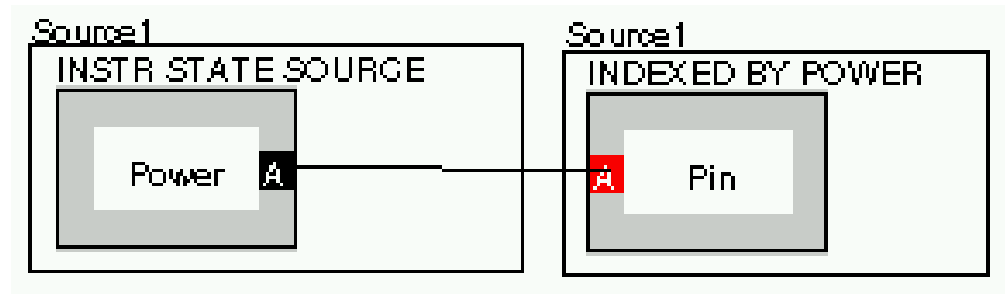


P1dB Step 4

- Save the second array, Source 1 power, also indexed by Source 1 Power

Index, Pin

1,	-30
2,	-29
3,	-28
4,	-27
5,	-26
6,	-25
7,	-24
8,	-23
9,	-22
10,	-21
11,	-20

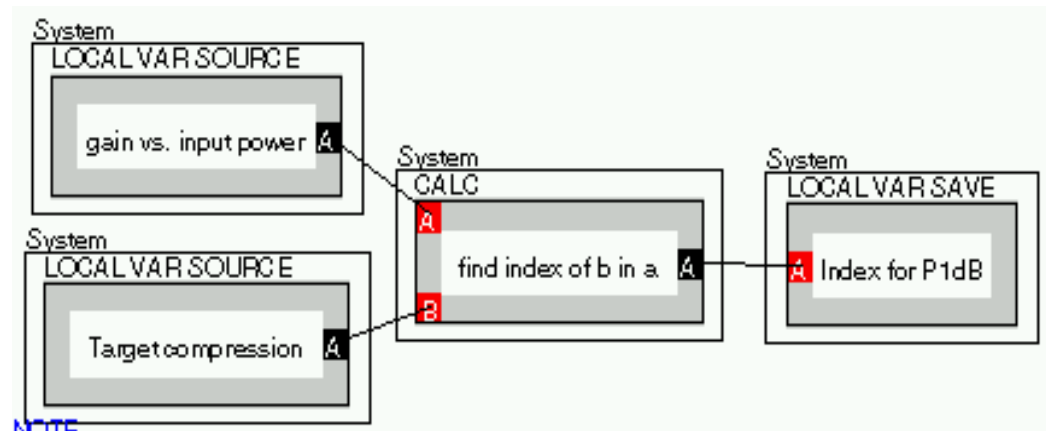




P1dB Step 5

- Find fractional index for P1dB (9 dB)
- This is an index of approximately 7.2

<i>Index, Gain</i>	
1,	10
2,	10
3,	10
4,	10
5,	10
6,	9.7
7,	9.2
8,	8.4
9,	7.5
10,	6.5
11,	5.5



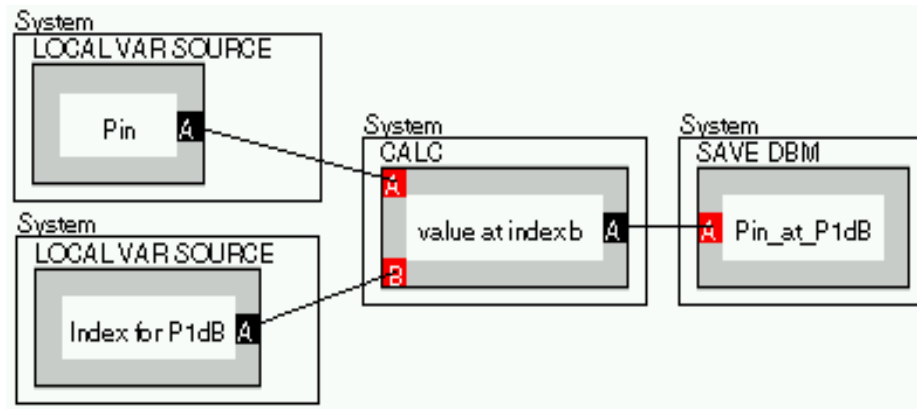


P1dB Step 6

- Extract Pin for that index. (~ -23.8 dBm)

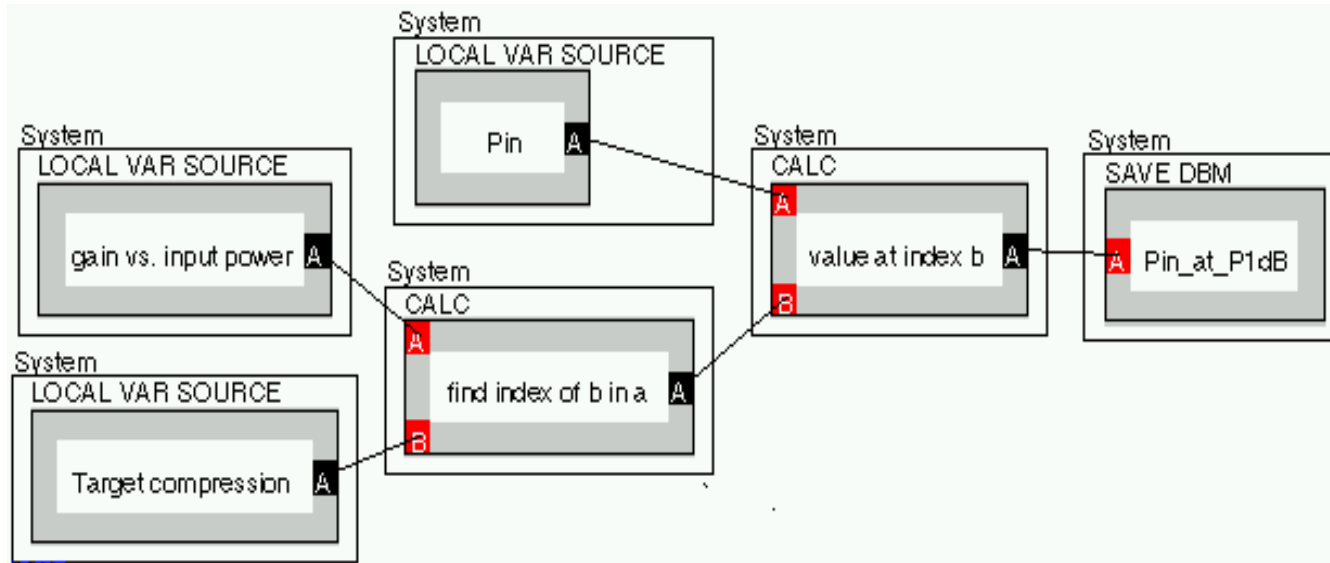
Index, Pin

1	-30
2	-29
3	-28
4	-27
5	-26
6	-25
7	-24
8	-23
9	-22
10	-21
11	-20





P1db Calculation





Measuring Noise Figure

- Set RF Source 1 to Device Input Freq.
- Set Receive Attenuation to 0 dB
- Set IF Filter Bandwidth to wide/4 MHz
- Set IF Gain for Hot Noise Measurement
System Automatically sets IF Gain 6 dB
Higher for Cold Noise Measurement



Noise Figure Measurement

The screenshot shows the ROOS INSTRUMENTS software interface for Noise Figure Measurement. The window title is "GSMNF2_V". The menu bar includes File, Edit, Test Plan, Tester, Limits, Options, Help, and Debug. The main area displays a list of tests in red text, with the selected test "Test: Noise Figure Max Gain@942_38_0_256" highlighted in black. To the right of the test list are three green buttons: Compile, Run, and Repeat. Below the test list is a control panel with several sections:

- Receiver:** IF GAIN (38)
- Source1:** RF STATE (OFF)
- Source1:** FREQUENCY (942.5 Mhz)
- System:** AVERAGES (256)
- Testhead:** REC ATTENUATION (0db)
- StaticDigital:** DB 1 (on)
- StaticDigital:** DB 2 (on)
- noiseFigure MEAS:** Noise Figure (A)
- System SAVE LOG:** NF_max@942_38_0_256 (A)

ROOS INSTRUMENTS



Expanded Noise Figure Measurement

- Set RF Source 1 to Device Input Freq.
- Set Receive Attenuation to 0 dB
- Set IF Filter Bandwidth to wide/4 MHz
- Set IF Gain for Hot Noise Measure
- Set IF Gain **+6,+12** or **+18** dB higher for Cold Noise Measurement



Expanded Noise Figure Calculating Device Noise Figure

- $F_1 = F_{12} - (F_2 - 1)/G_1$
- F_1 = Device Noise Figure
- F_2 = Tester/Second Stage Noise Figure
- F_{12} = Measured Noise Figure
- G_1 = Device Noise Gain



Expanded Noise Figure

GSMNF2_V

File Edit Test Plan Tester Limits Options Help Debug

Test: Pout Mid Gain_-25_dBm_40_20
Test: S11 & S21 Max@925_40_10
Test: S11 & S21 Max@942.5_40_10
Test: S11 & S21 Max@960_40_10
Test: S22 only Max Gain
Test: Noise Figure Mid Gain@942_50_56_0_256 Expanded
Test: Noise Figure Mid Gain@942_50_0_256
Test: Noise Figure Max Gain@942_38_56_0_256 Expanded
Test: Noise Figure Max Gain@942_38_0_256
Test: Noise Figure Max Gain@942_38_38_0_256 Old

Compile
Run
Repeat

MEASURE

Receiver IF GAIN 56
noiseFigure MEAS NfCold Noise A

MEASURE

Receiver IF GAIN 38
noiseFigure MEAS NfHot Noise A

noiseFigure MEAS Input ENR A

System CALC Noise Figure, cold, hot enr A
noiseFigure MEAS 2nd Stage Noise Figure A
noiseFigure MEAS Port Noise Gain A
System CALC Noise Gain, cold, hot, enr A

System CALC a - b A
System CALC a / b A
System CALC a / b A

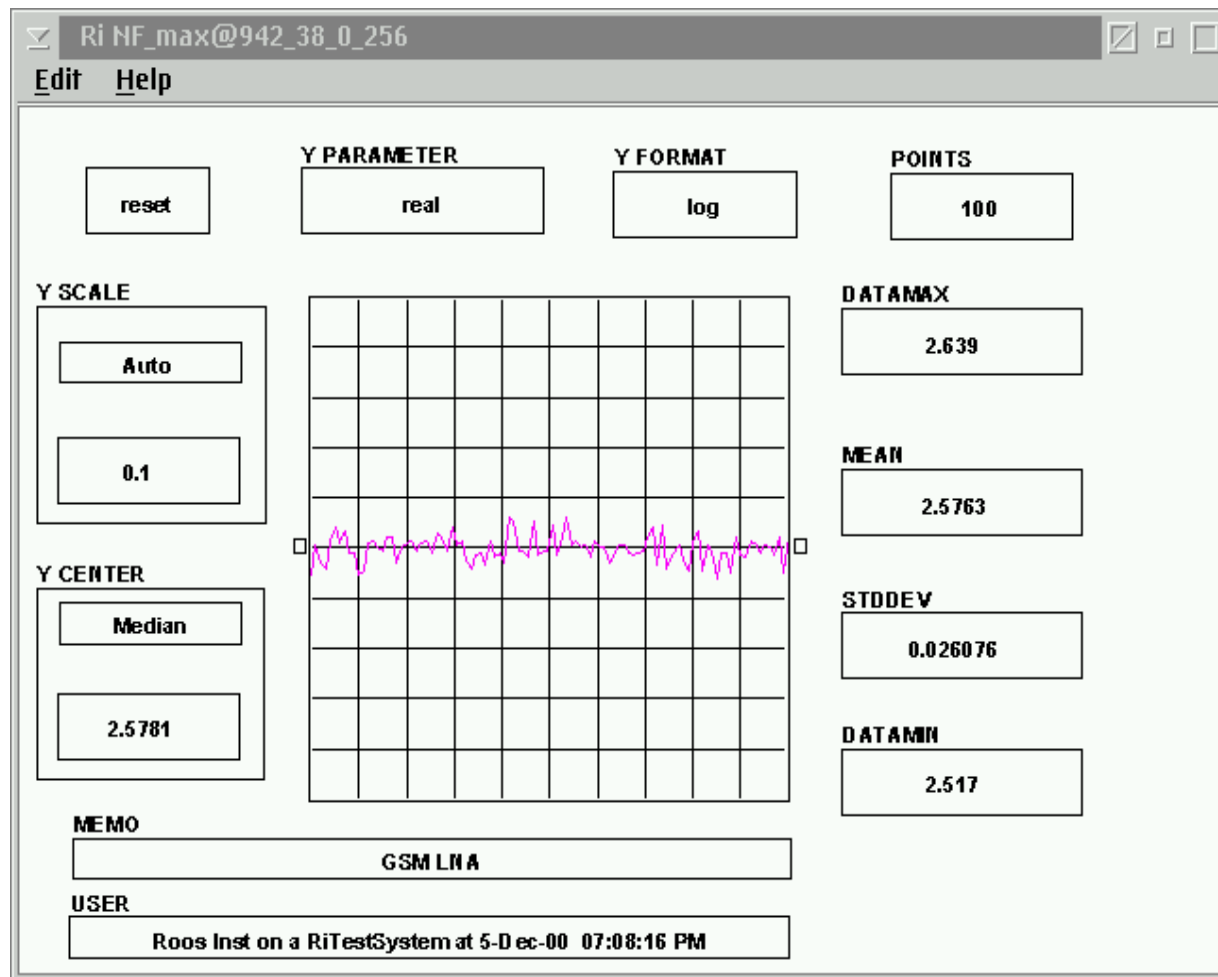
Receiver IF GAIN 38
StaticDigital DB 1 on
System AVERAGES 256
Source1 RF STATE OFF
StaticDigital DB 2 on
Testhead REC ATTENUATION 0db
Source1 FREQUENCY 942.5 Mhz

SAVE LOG NF_max_expand@942_38_56_0_256

NOTE

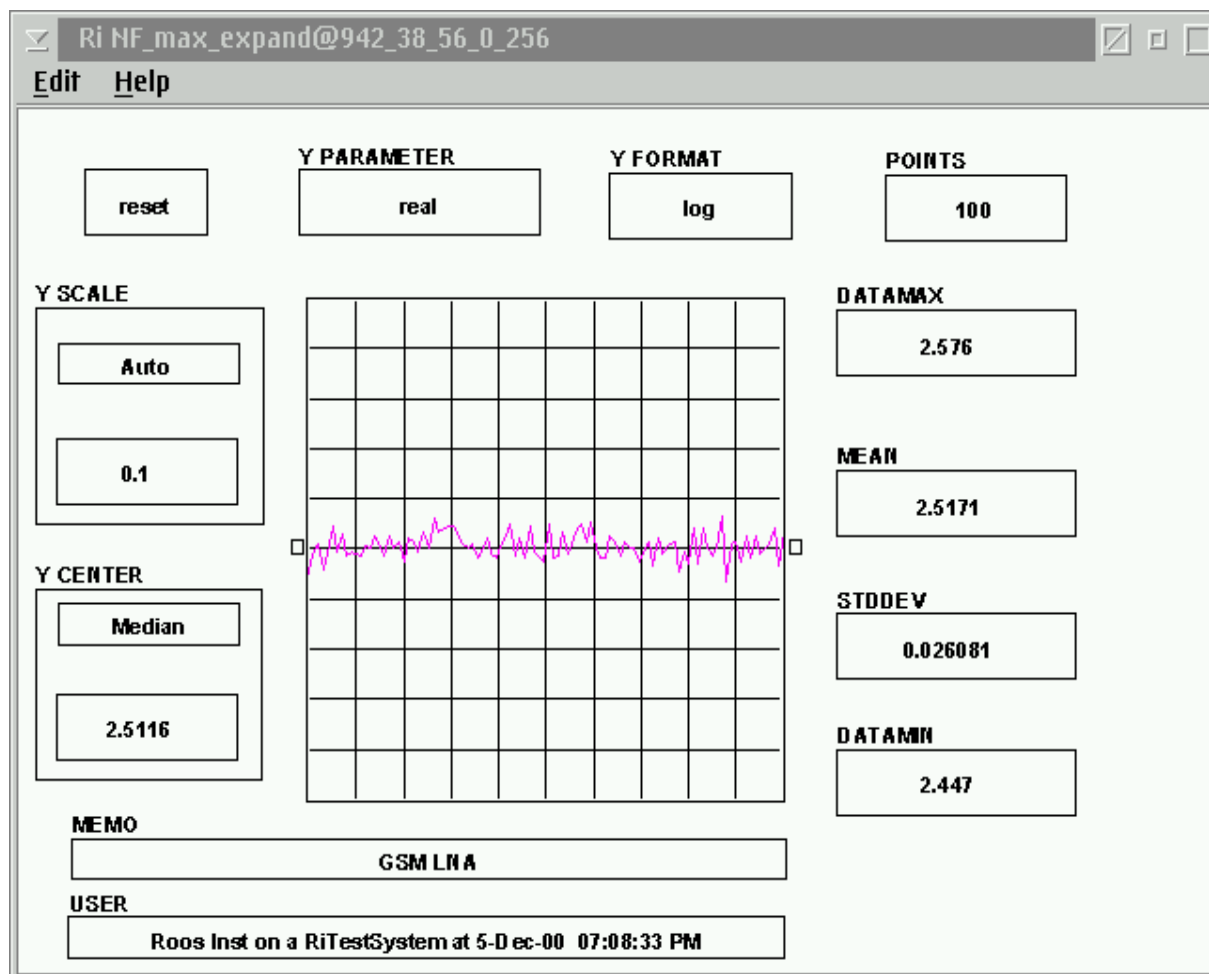


Noise Figure Measurement IF Gain +6 dB higher for Cold





Expanded Noise Figure IF Gain set for Hot & Cold





Example LNA Test Plan

CASSINI Simulator - Examine Test Plan

Test Plan Settings

Global Defaults

Disconnect Settings

Connect Sequence

Test Section: Current Tests

Conditional Statement

Section Defaults

Test: Igq

Test: IDD

Test Section: RF Tests

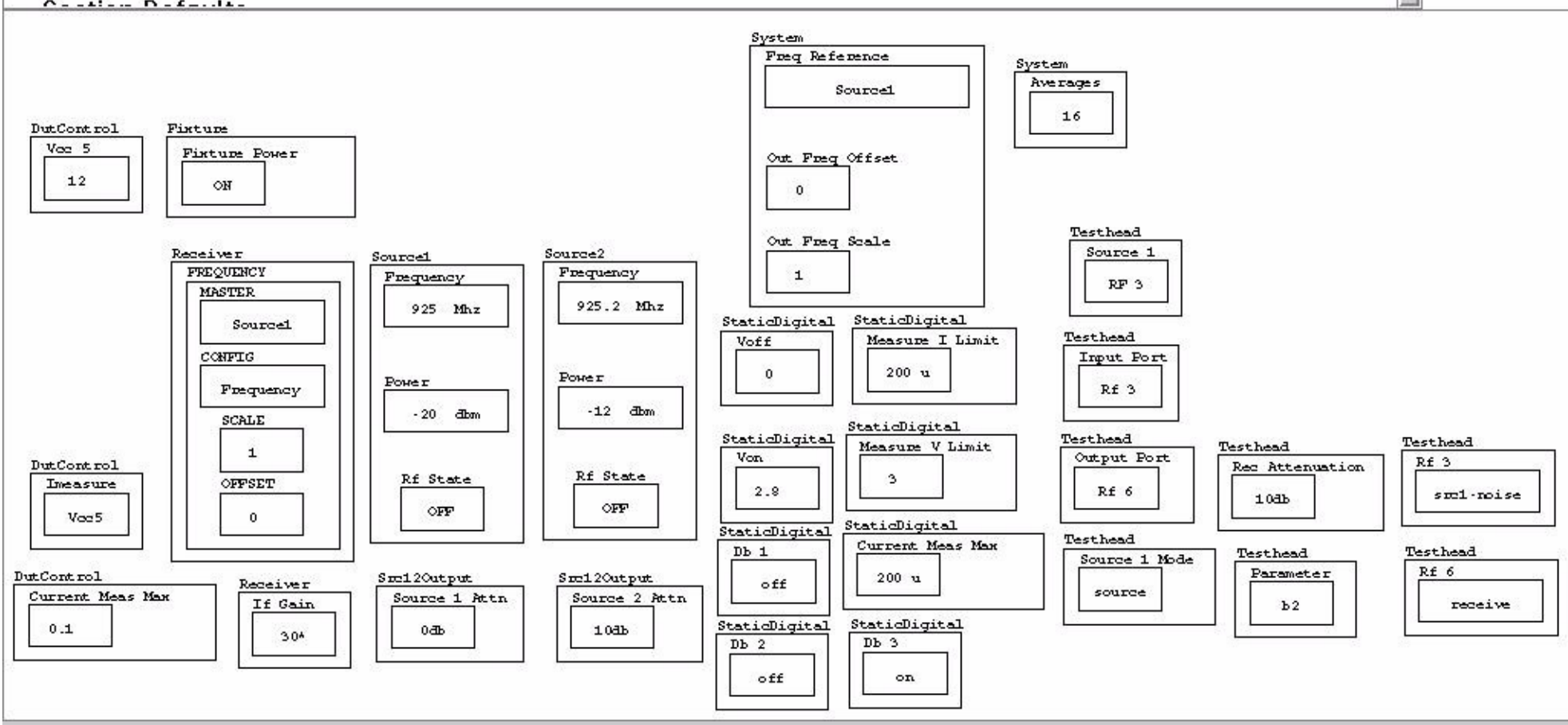
Conditional Statement

Section Defaults

Compile

Run

Repeat



LNA_example_revD

File Edit Test Plan Tester Limits Options Help Debug

Test Plan Settings

- Global Defaults
- Disconnect Settings**
- Connect Sequence

Test Section: Current Tests

- Conditional Statement
- Section Defaults
- Test: Igcq
- Test: IDD

Test Section: RF Tests

- Conditional Statement
- Section Defaults

Compile

Run

Repeat

Source1

Rf State

OFF

Source2

Rf State

OFF

StaticDigital

Db 2

off

StaticDigital

Db 3

off

DutControl

Vcc 5

0

NOTE

LNA_example_revD

File Edit Test Plan Tester Limits Options Help Debug

Test Plan Settings

- Global Defaults
- Disconnect Settings
- Connect Sequence**

Test Section: Current Tests

- Conditional Statement
- Section Defaults
- Test: Igcq
- Test: IDD

Test Section: RF Tests

- Conditional Statement
- Section Defaults

Compile

Run

Repeat

DutControl

Vcc 5

2.7

System

Sequence Delay

5000

StaticDigital

Db 2

on

StaticDigital

Db 3

on

Source1

Rf State

ON

Source2

Rf State

ON

NOTE

LNA_example_revD

File Edit Test Plan Tester Limits Options Help Debug

Test Plan Settings
Global Defaults
Disconnect Settings
Connect Sequence

Test Section: Current Tests
Conditional Statement
Section Defaults
Test: Igcq
Test: IDD

Test Section: RF Tests
Conditional Statement
Section Defaults

Compile
Run
Repeat

Receiver
Frequency
925 Mhz

Source1
Rf State
OFF

Source2
Rf State
OFF

NOTE

The screenshot shows a software window titled 'LNA_example_revD' with a menu bar (File, Edit, Test Plan, Tester, Limits, Options, Help, Debug). The main area is divided into sections: 'Test Plan Settings' (Global Defaults, Disconnect Settings, Connect Sequence), 'Test Section: Current Tests' (Conditional Statement, Section Defaults, Test: Igcq, Test: IDD), and 'Test Section: RF Tests' (Conditional Statement, Section Defaults). On the right, there are buttons for 'Compile', 'Run', and 'Repeat'. Below the settings, three components are displayed: 'Receiver' with a 'Frequency' of '925 Mhz', 'Source1' with 'Rf State' set to 'OFF', and 'Source2' with 'Rf State' set to 'OFF'. A 'NOTE' label is at the bottom left.

LNA_example_revD

File Edit Test Plan Tester Limits Options Help Debug

Test Plan Settings
Global Defaults
Disconnect Settings
Connect Sequence

Test Section: Current Tests
Conditional Statement
Section Defaults

Test: Igcq
Test: IDD

Test Section: RF Tests
Conditional Statement
Section Defaults

Compile
Run
Repeat

StaticDigital
Measure V Force
3

StaticDigital
Measure Mode
I meas

System
Averages
32

StaticDigital
Measure Pin
DB2

StaticDigital
Current Meas Max
200 u

StaticDigital
MEAS
Current A

System
Save Amps
Igc

StaticDigital
Db 2
open

StaticDigital
Measure I Limit
200 u

LNA_example_revD

File Edit Test Plan Tester Limits Options Help Debug

Test Plan Settings
Global Defaults
Disconnect Settings
Connect Sequence
Test Section: Current Tests
Conditional Statement
Section Defaults
Test: Igcq
Test: IDD
Test Section: RF Tests
Conditional Statement
Section Defaults

Compile
Run
Repeat

The diagram shows a test plan configuration with the following components and connections:

- StaticDigital Db 1**: Set to `off`.
- StaticDigital Db 2**: Set to `on`.
- DutControl Current Meas Max**: Set to `0.1`.
- DutControl Imeasure**: Set to `Vcc5`.
- System Averages**: Set to `64`.
- DutControl MEAS**: Contains a **Current A** block.
- System Save Amps**: Contains an **IDD A** block.

A connection line links the **Current A** block in the MEAS block to the **IDD A** block in the Save Amps block.

LNA_example_revD

File Edit Test Plan Tester Limits Options Help Debug

Conditional Statement
Section Defaults
Test: Igcq
Test: IDD
Test Section: RF Tests
Conditional Statement
Section Defaults
Test: Gain and Input Return Loss
Test: S22 only
Test: Gain Flatness
Test: Calc Gain Flatness
Test: Target Gain

Compile
Run
Repeat

Source1
Rf State
ON

StaticDigital
Db 2
on

The image shows a software window titled "LNA_example_revD" with a menu bar containing "File", "Edit", "Test Plan", "Tester", "Limits", "Options", "Help", and "Debug". The main area is divided into two sections. The upper section is a tree view showing a hierarchy of test sections: "Conditional Statement", "Section Defaults", "Test: Igcq", "Test: IDD", "Test Section: RF Tests", "Conditional Statement", "Section Defaults" (highlighted with a black background and a mouse cursor), "Test: Gain and Input Return Loss", "Test: S22 only", "Test: Gain Flatness", "Test: Calc Gain Flatness", and "Test: Target Gain". To the right of this tree view are three buttons: "Compile", "Run", and "Repeat". The lower section of the window displays two test components. The first is labeled "Source1" and contains a sub-section "Rf State" with the value "ON". The second is labeled "StaticDigital" and contains a sub-section "Db 2" with the value "on".

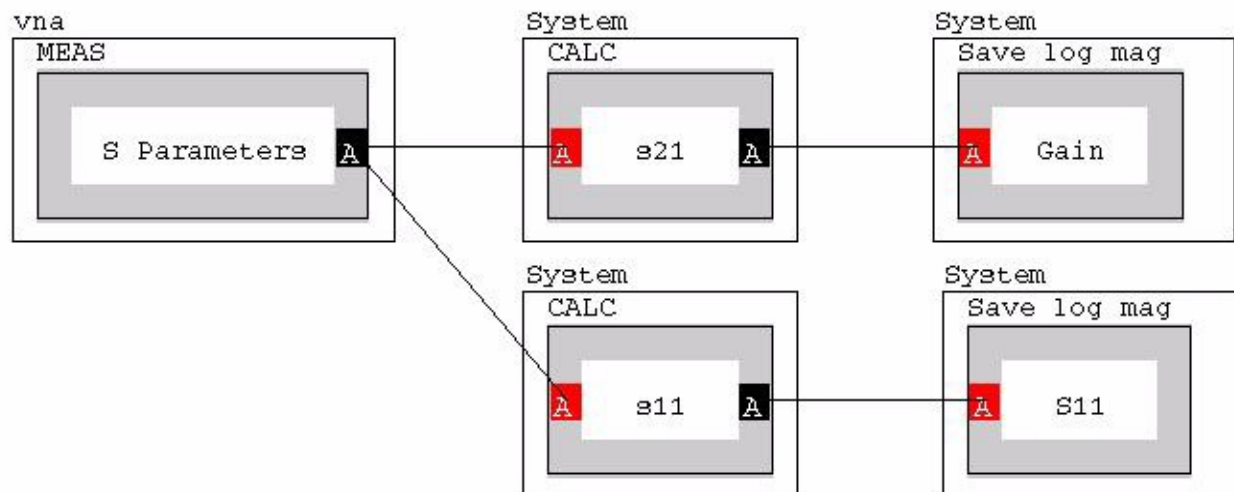
LNA_example_revD

File Edit Test Plan Tester Limits Options Help Debug

Conditional Statement
Section Defaults
Test: Igq
Test: IDD

Test Section: RF Tests
Conditional Statement
Section Defaults
Test: Gain and Input Return Loss
Test: S22 only
Test: Gain Flatness
Test: Calc Gain Flatness
Test: Target Gain

Compile
Run
Repeat



LNA_example_revD

File Edit Test Plan Tester Limits Options Help Debug

Conditional Statement
Section Defaults
Test: Igcq
Test: IDD

Test Section: RF Tests
Conditional Statement
Section Defaults
Test: Gain and Input Return Loss
Test: S22 only
Test: Gain Flatness
Test: Calc Gain Flatness
Test: Target Gain

Compile
Run
Repeat

Source1

Power

-12 dbm

Testhead

Source 1

Load

Testhead

Load State

source 1

Testhead

Input Port

Rf 6

Testhead

Output Port

Rf 6

vna

MEAS

S11 Only A

System

Save log mag

A S22_rev_path

LNA_example_revD

File Edit Test Plan Tester Limits Options Help Debug

Conditional Statement
Section Defaults
Test: Igcq
Test: IDD

Test Section: RF Tests
Conditional Statement
Section Defaults
Test: Gain and Input Return Loss
Test: S22 only
Test: Gain Flatness
Test: Calc Gain Flatness
Test: Target Gain

Compile
Run
Repeat

Source1
Frequency
925 Mhz

Source1
Frequency
942.5 Mhz

Source1
Frequency
960 Mhz

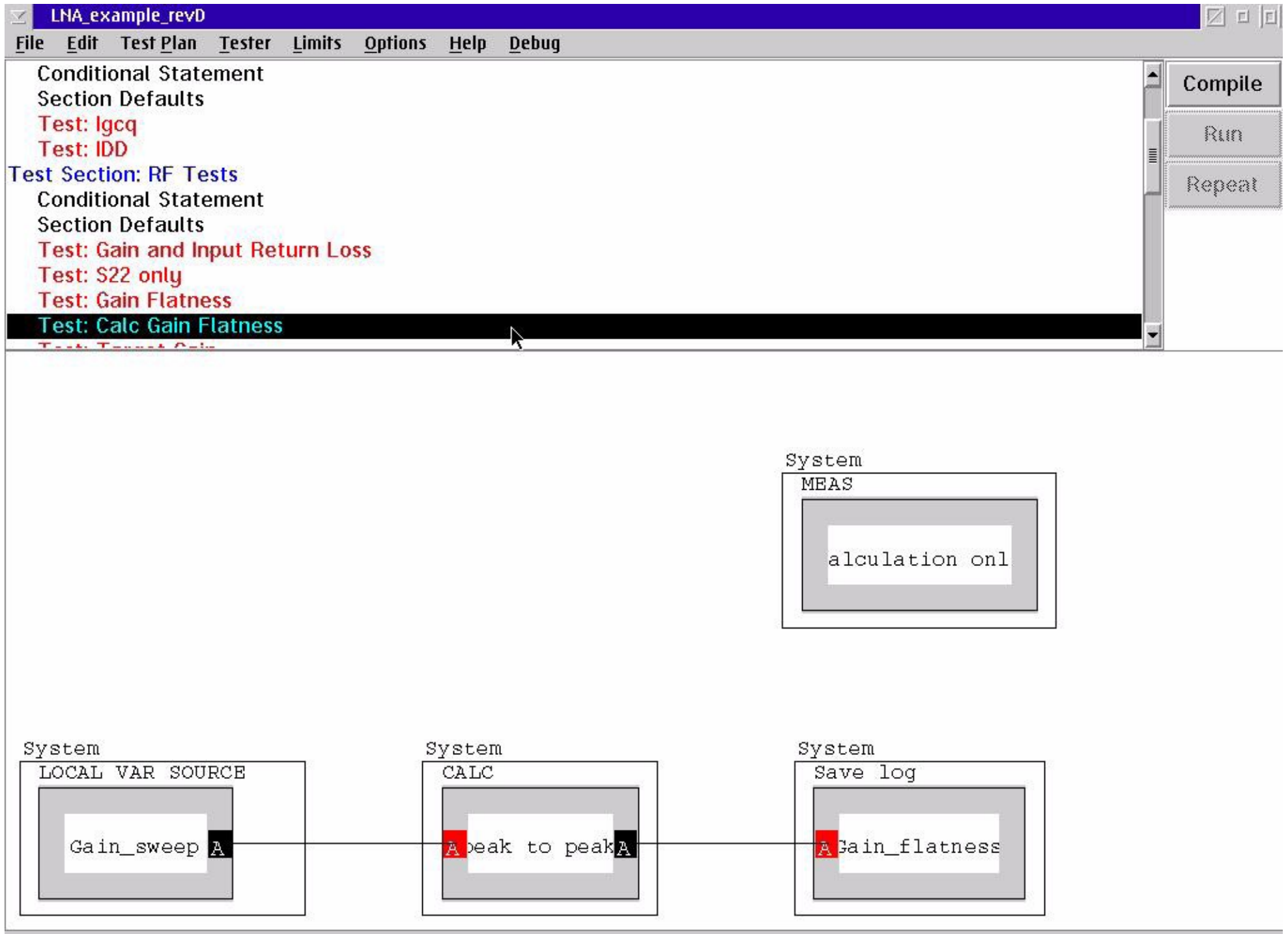
vna
MEAS
S Parameters A

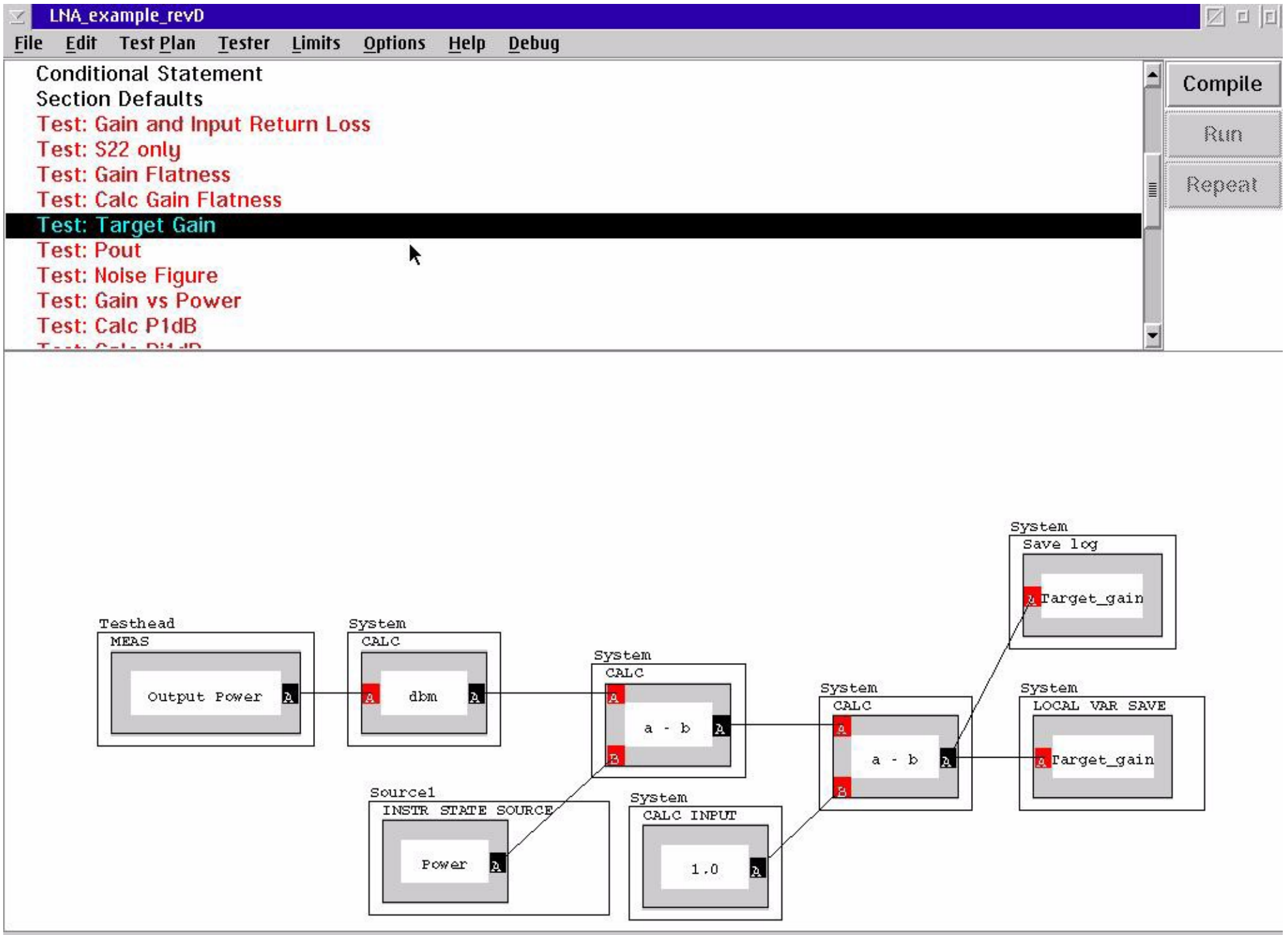
System
CALC
s21 A

System
CALC
magnitude (db) A

System
LOCAL VAR SAVE
Gain_sweep A

System
Save log
Gain_sweep A





LNA_example_revD

File Edit Test Plan Tester Limits Options Help Debug

Conditional Statement
Section Defaults
Test: Gain and Input Return Loss
Test: S22 only
Test: Gain Flatness
Test: Calc Gain Flatness
Test: Target Gain
Test: Pout
Test: Noise Figure
Test: Gain vs Power
Test: Calc P1dB
Test: Calc P1dB

Compile
Run
Repeat

Source1
Power
-12 dbm

Testhead
MEAS
Output Power A

System
CALC
A dbm A

System
LOCAL VAR SAVE
A Pout

```
graph LR; Source1[Source1: Power -12 dbm] --> Testhead[Testhead: MEAS Output Power A]; Testhead --> System1[System: CALC A dbm A]; System1 --> System2[System: LOCAL VAR SAVE A Pout];
```

LNA_example_revD

File Edit Test Plan Tester Limits Options Help Debug

Conditional Statement
Section Defaults
Test: Gain and Input Return Loss
Test: S22 only
Test: Gain Flatness
Test: Calc Gain Flatness
Test: Target Gain
Test: Pout
Test: Noise Figure
Test: Gain vs Power
Test: Calc P1dB
Test: Calc P1dB

Compile
Run
Repeat

Receiver
If Gain
50

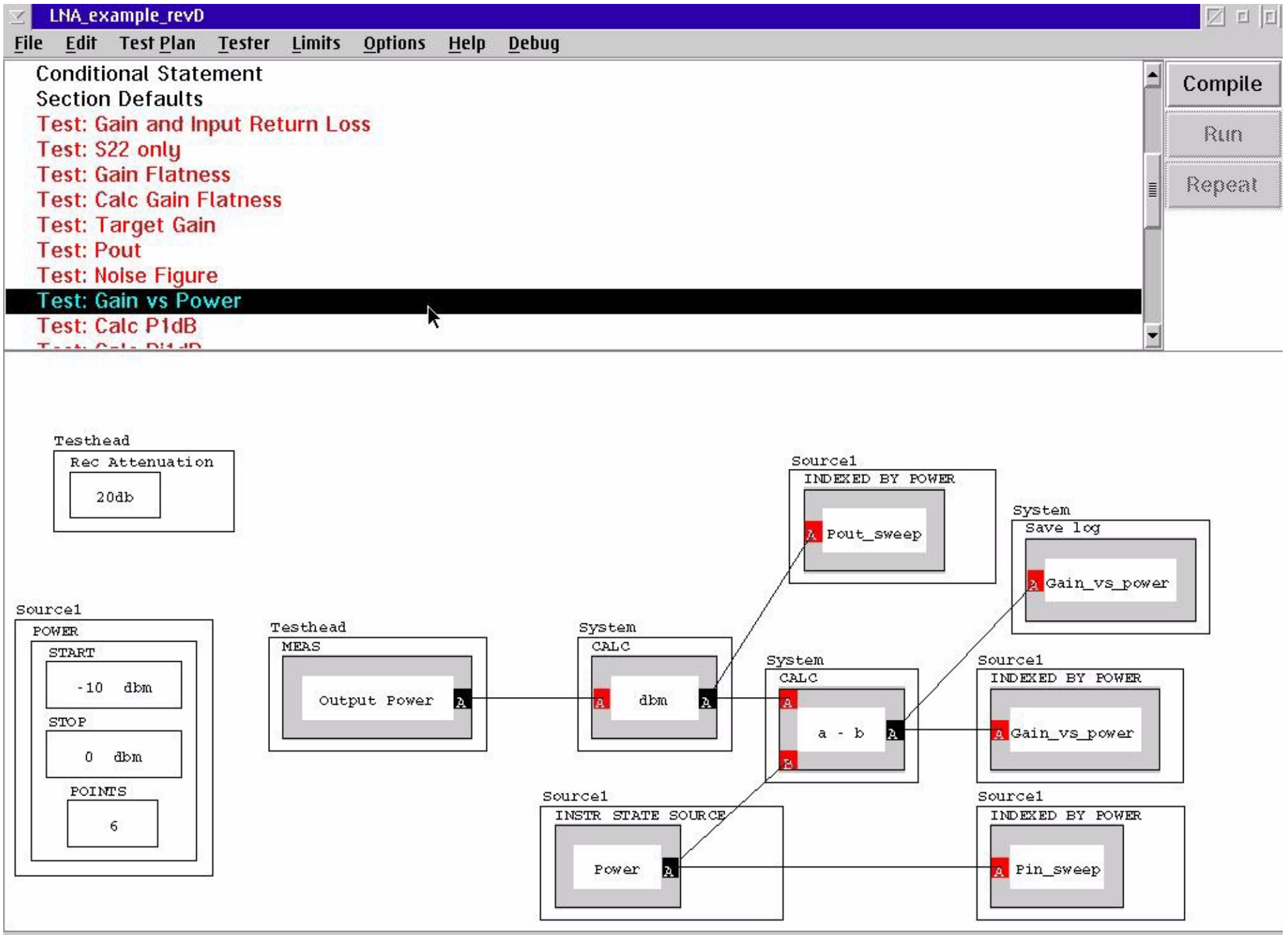
Source1
Rf State
OFF

System
Averages
128

Testhead
Rec Attenuation
0db

noiseFigure
MEAS
Noise Figure A

System
Save log
A NF

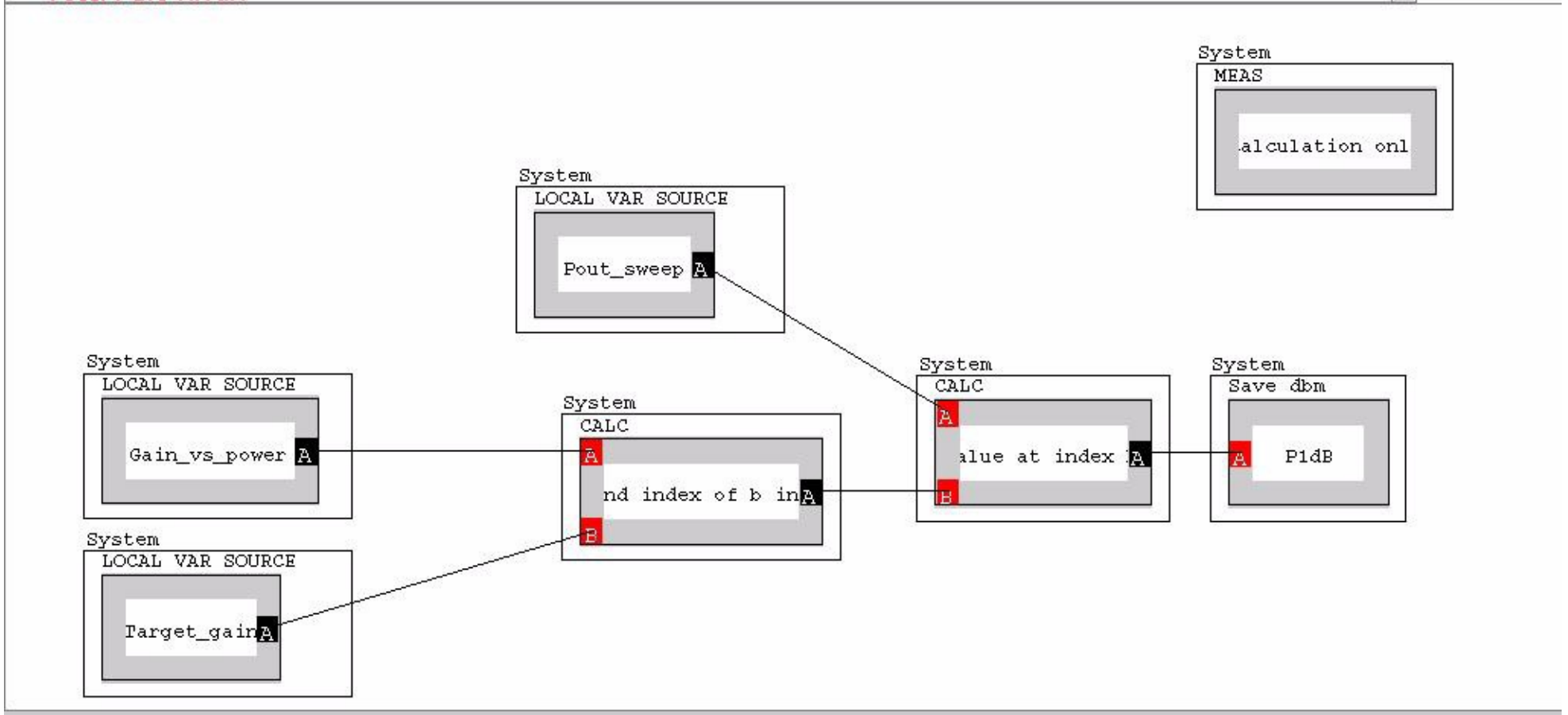


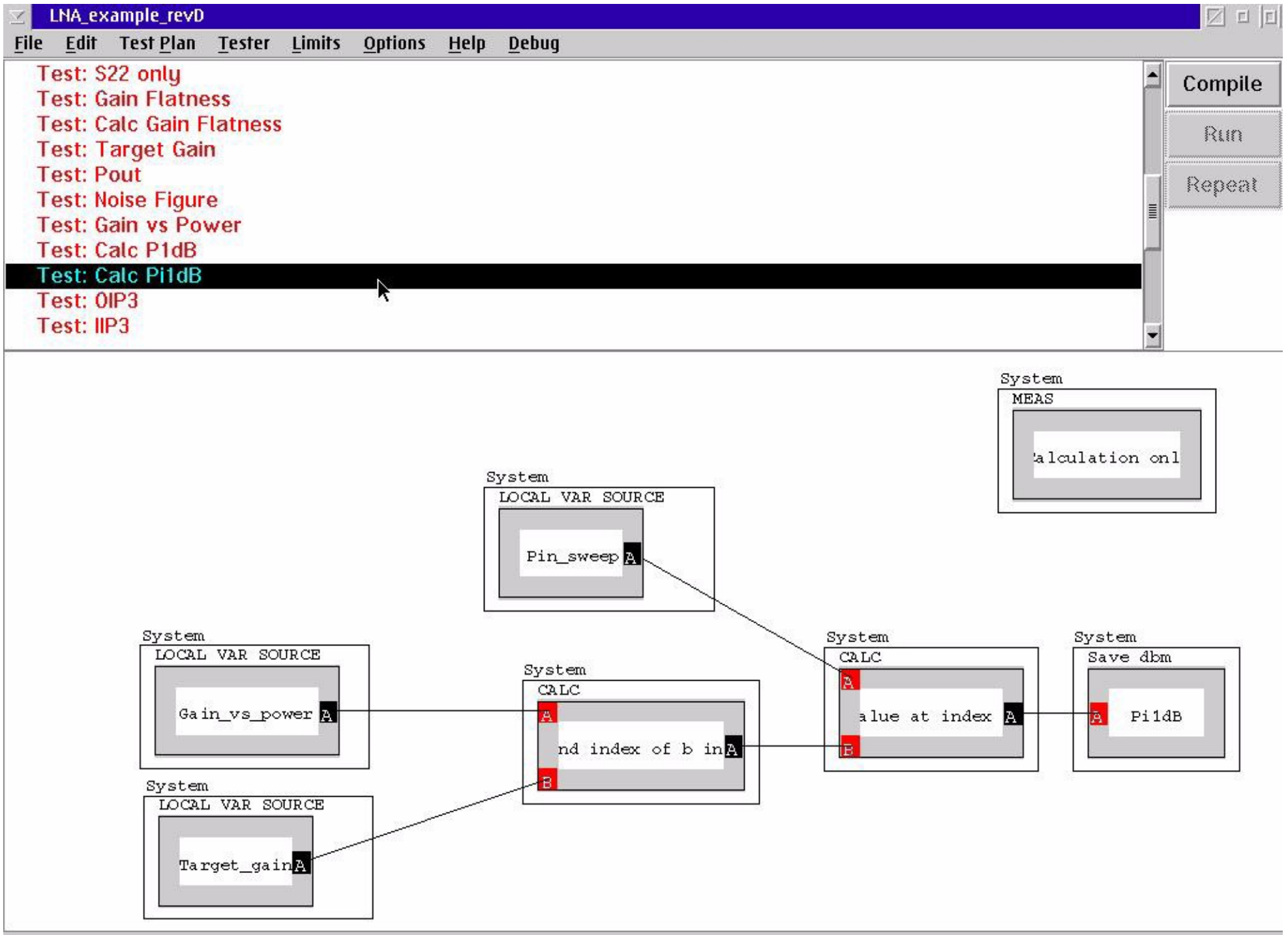
LNA_example_revD

File Edit Test Plan Tester Limits Options Help Debug

Conditional Statement
 Section Defaults
 Test: Gain and Input Return Loss
 Test: S22 only
 Test: Gain Flatness
 Test: Calc Gain Flatness
 Test: Target Gain
 Test: Pout
 Test: Noise Figure
 Test: Gain vs Power
Test: Calc P1dB
 Test: Calc P1dB

Compile
 Run
 Repeat



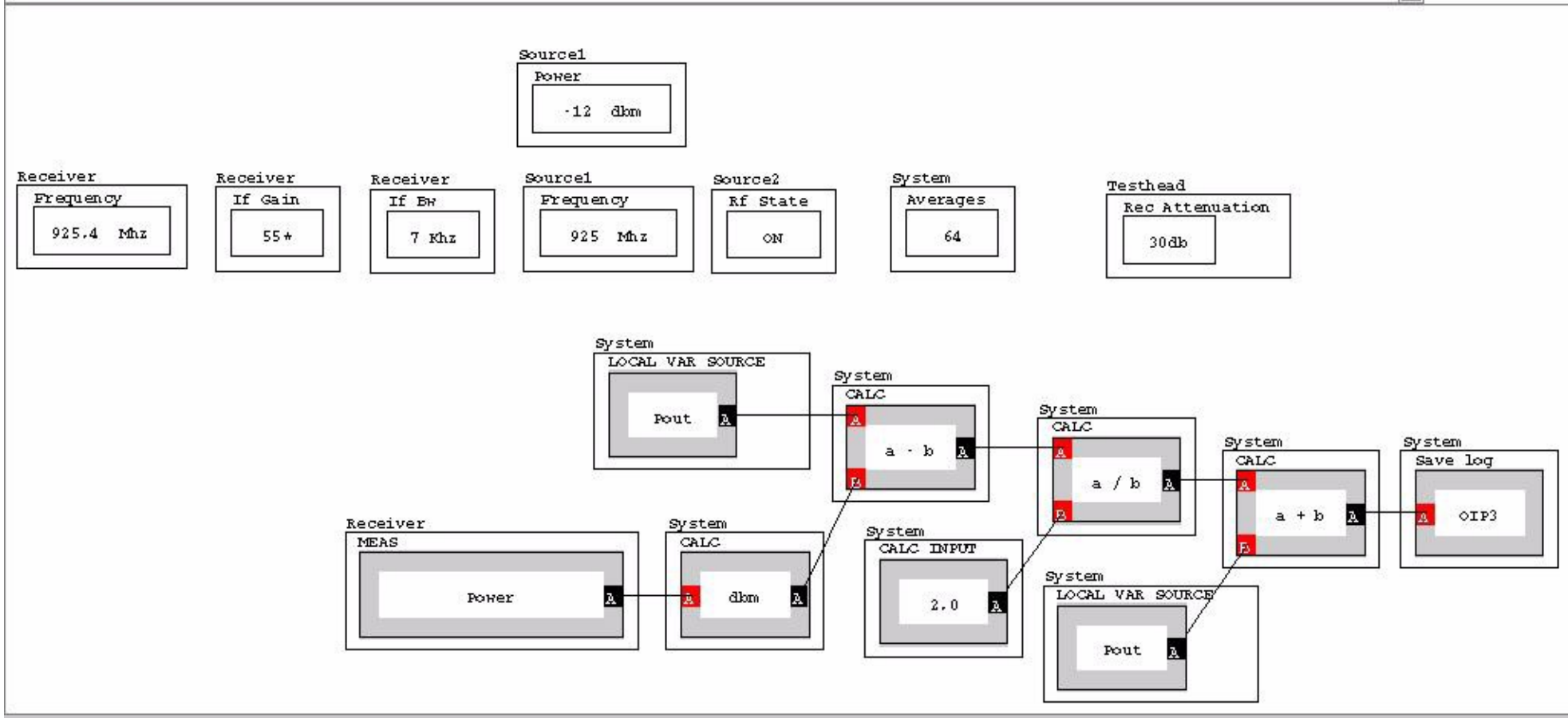


LNA_example_revD

File Edit Test Plan Tester Limits Options Help Debug

Test: S22 only
 Test: Gain Flatness
 Test: Calc Gain Flatness
 Test: Target Gain
 Test: Pout
 Test: Noise Figure
 Test: Gain vs Power
 Test: Calc P1dB
 Test: Calc P1dB
Test: OIP3
 Test: IIP3

Compile
 Run
 Repeat

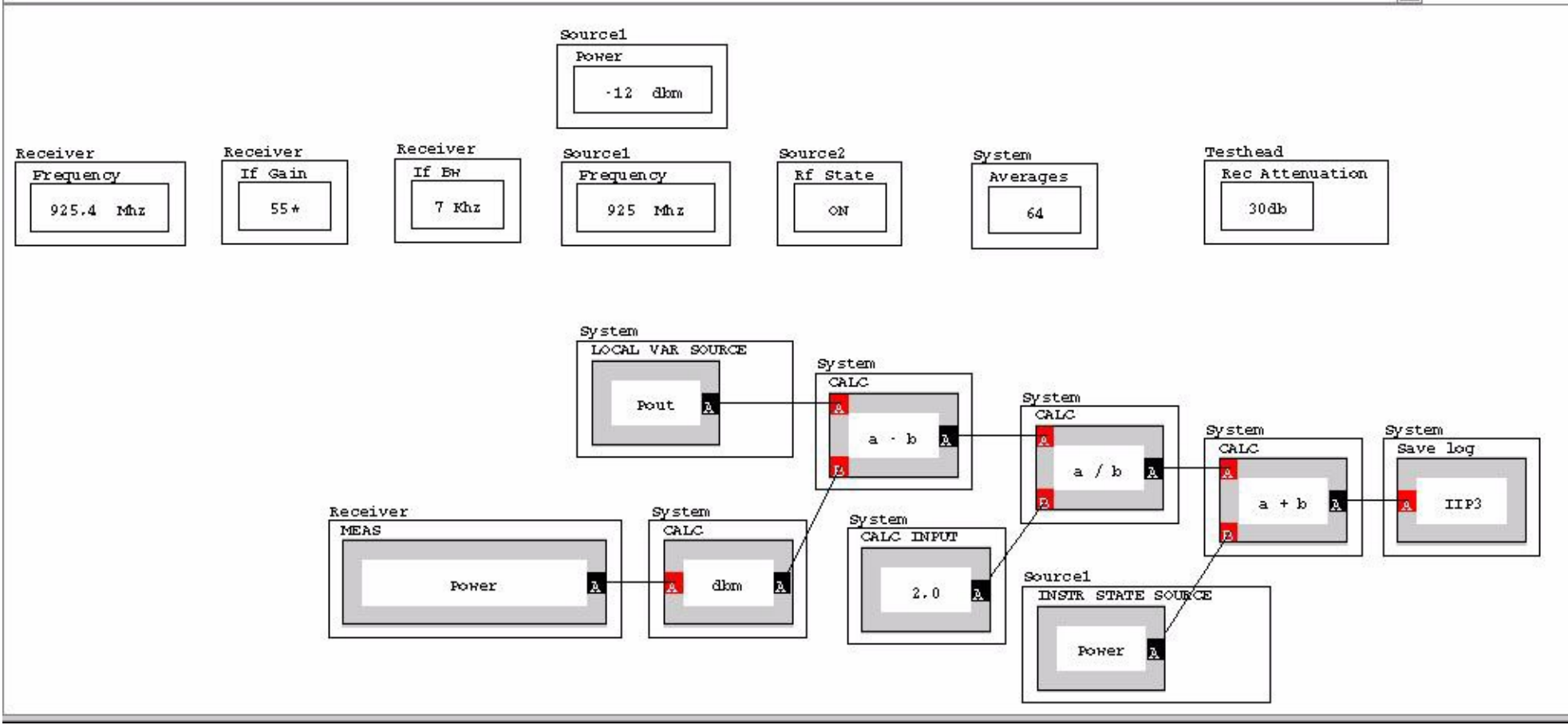


LNA_example_revD

File Edit Test Plan Tester Limits Options Help Debug

Test: S22 only
 Test: Gain Flatness
 Test: Calc Gain Flatness
 Test: Target Gain
 Test: Pout
 Test: Noise Figure
 Test: Gain vs Power
 Test: Calc P1dB
 Test: Calc P1dB
 Test: OIP3
Test: IIP3

Compile
 Run
 Repeat





Writing a LNA Test Plan - Lab D

- Get into Groups of Three
- Each will take turns performing the lab
- One types, one reads, one uses mouse



LNA Test Plan Lab

Develop 3rd Harmonic

- RF Input Level = -5 dBm
- RF Input Frequency = 960 MHz
- 3rd Harmonic Spec. Approx. -35 dBc
- Device Gain Approx. +10 dB
- Calc 3rd Harmonic in dBc
- Extra Credit:
 - Find 3rd Harmonic at +5 dBm Out



PA Tests

- DC Current & PAE
- S11, S21, S12 & S22
- Noise Figure
- P1dB
- Intermodulation Distortion
- Harmonics
- ACPR @ Specified Output Power



PA Test Plan Measurements

- Gain
- P1dB
- Fixed Pout
- IM3
- Leakage Current
- ACPR/ACLR
- Efficiency



PA Test Considerations

- Set Up DMSG in Global Defaults
- Use SRC12/Aux Pwr not Aux SRC/Pwr for sweep
- SRC12/Aux Pwr is Actually Attenuation
- Use RMS Power for Modulated Tones
- Characterize Noise BW of IF Filters for Modulation Type
- Use DB Line for Leakage Current Measurement

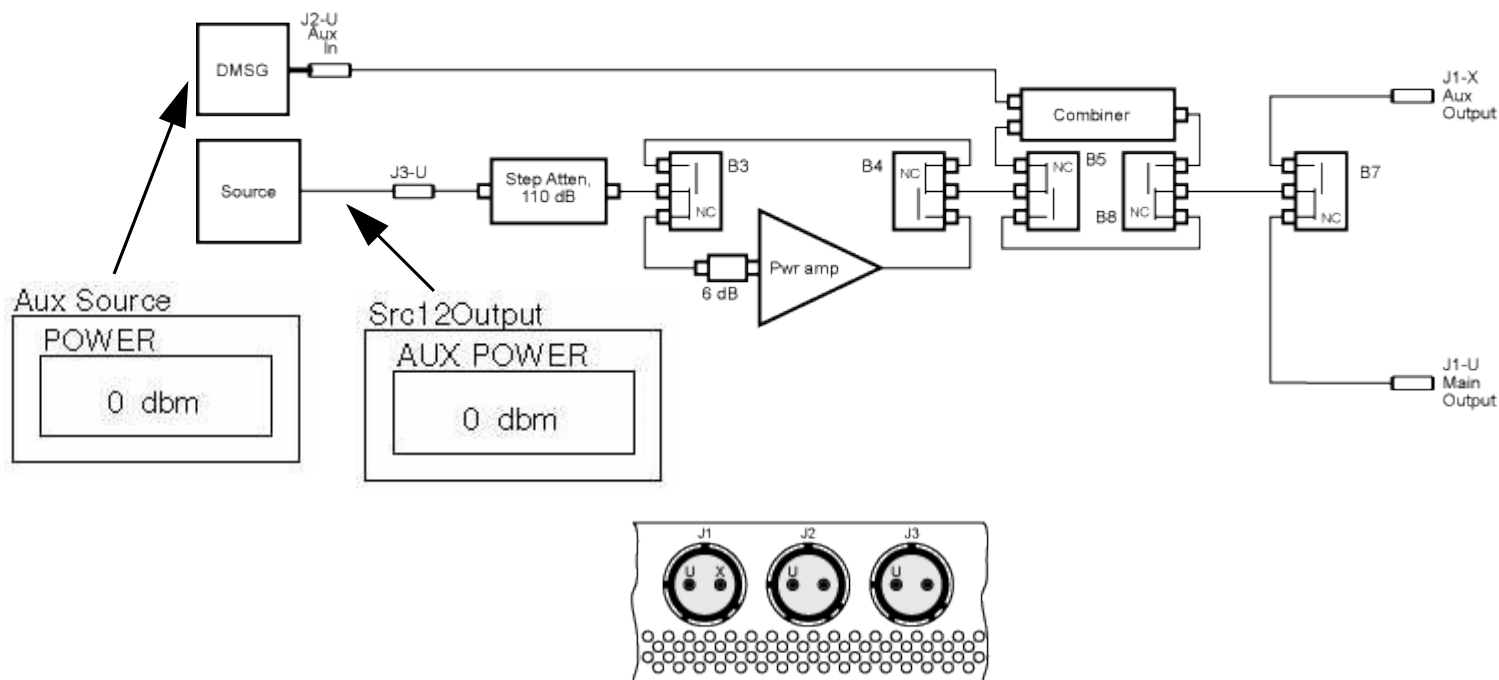


Aux Attenuator Path

Roos Instruments, Inc - Cassini
Block Diagram, Source/Amp Attenuator
RI8555A

2007-2-6

Copyright Roos Instruments, Inc.
Subject to change without notice



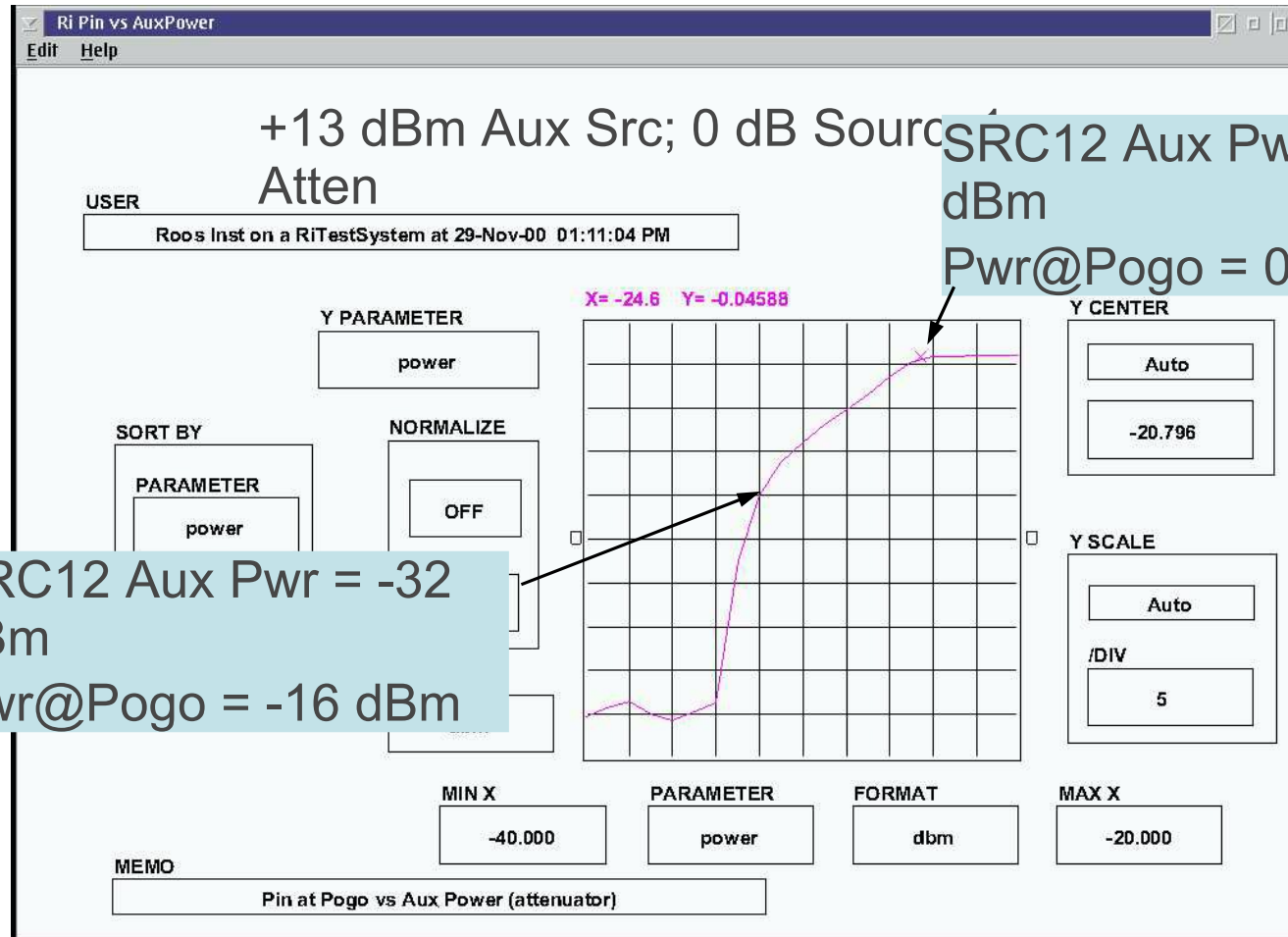


Src12 Aux Power

- Attenuator not Power
- Logarithmic Attenuation
- Approximately 13 dB Path Loss in 0 dB Attenuation State (DMSG to Pogo Ring)
- Effective Settings: SRC12/AuxPwr
 - -24 dBm = 13 dB path loss = 0 dB atten
 - -32 dBm = 29 dB path loss = 16 dB atten



Available vs. Src12/AuxPower



SRC12 Aux Pwr = -32 dBm
Pwr@Pogo = -16 dBm

SRC12 Aux Pwr = -24 dBm
Pwr@Pogo = 0 dBm



Aux Source Capabilities

- Anritsu MG3671B; +13 dBm max.
- Aux Src Only: 0 dBm @ Pogo
- With SRC1 Amp: Approximately +20 dBm @ Pogo
- CDMA, TDMA, PDC, GSM, TETRA, DECT



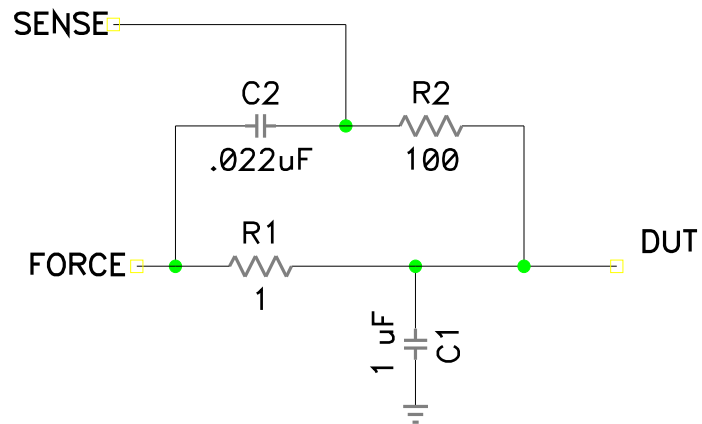
VI Loading

- Power VIs designed for $<0.1\mu\text{F}$
- 3 μSec settling, Faster than bench
- Some PA eval boards have higher values
- Design Dut boards appropriately
- If Dut must have $>1\mu\text{F}$ cap use following method



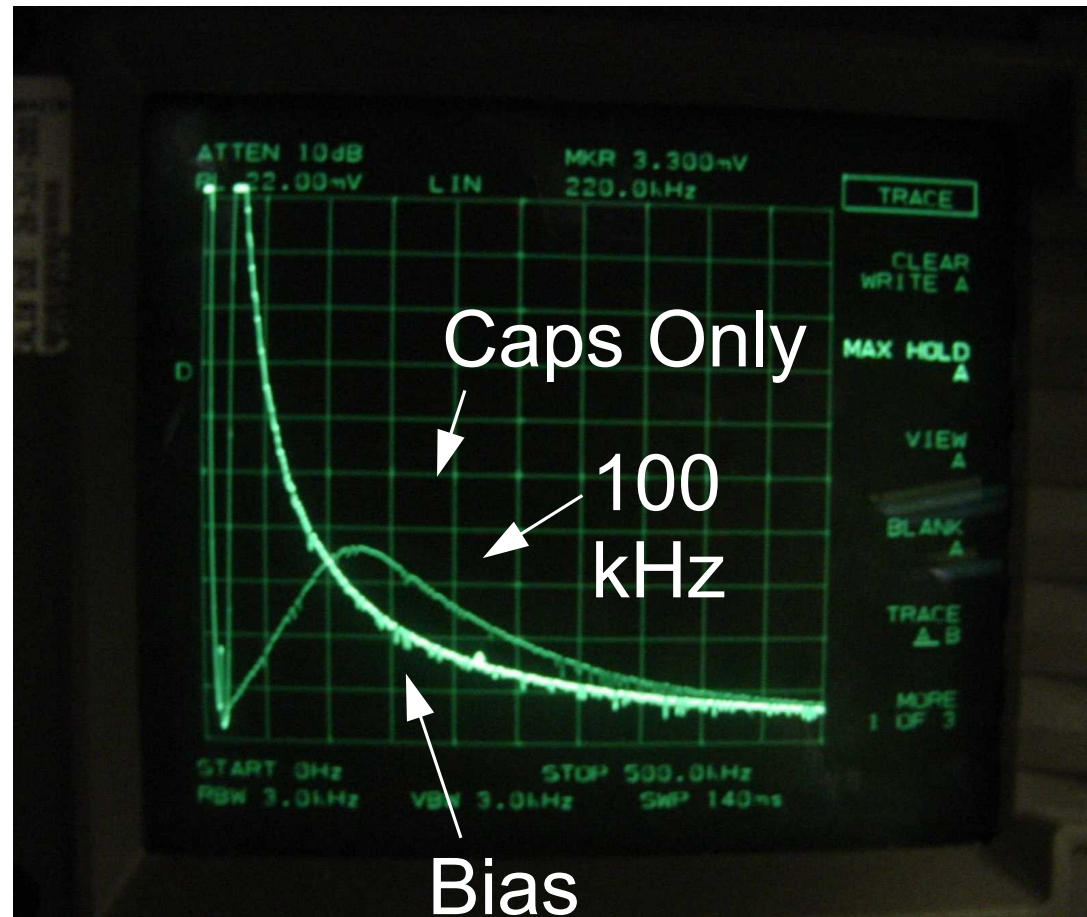
Loading Circuit

- C1 must be Ceramic (low R)
- R1, high watt; isolates Cap from VI





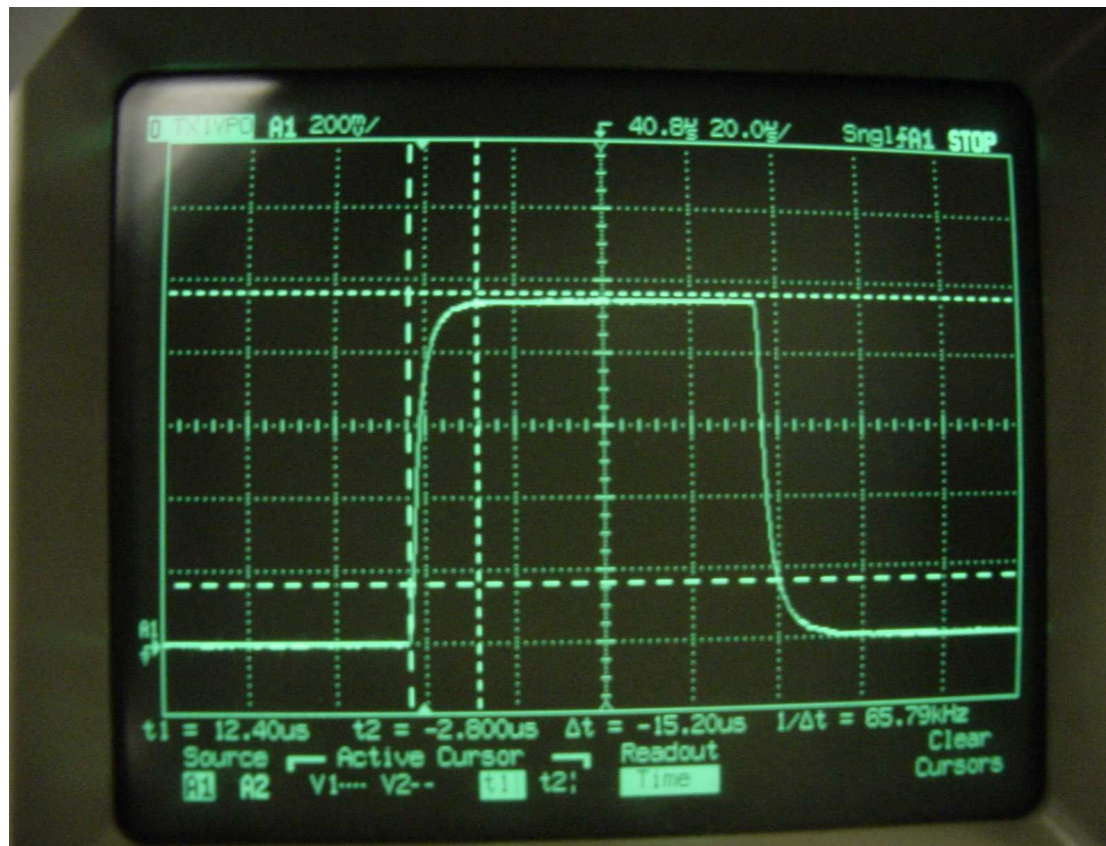
Circuit Frequency Response





Circuit Time Response

- 15 uSec Settling



ROOS INSTRUMENTS



Switching DC Supplies

- RI Supplies "Break before Make"
- Supplies for Special Measurements
- Power VI; High Current
- DB; Leakage Current
- Concerns:
 - Device Memory
 - Decoupling Capacitance
 - Test Order



Switching Mechanism

- DB 4 x 8 Matrix
 - Von
 - Voff
 - Open
 - Parametric Measure
- VI
 - On
 - Off



Make before Break

- Connect Two Supplies at a Time
- DB Compliance
 - Mode Switching
 - Current Limit Applies
- VI Compliance
 - Drop Voltage to Limit Current
- Pre and Post Measure Group



Leakage Current Measurements

OSCAR_C14_FM_SRC2

File Edit Test Plan Tester Limits Options Help Debug

<DISABLED>Conditional Statement
<DISABLED>Section Defaults
<DISABLED>Test: Total Chip Leakage
Test Section: Junk (Unoptimized)
Conditional Statement
Section Defaults
Test: Total Chip Leakage
Test Section: DC Quiescent Tests (Unoptimized)
Conditional Statement
Section Defaults

PRE MEAS

StaticDigital MEASURE V FORCE 3.4	StaticDigital MEASURE PIN DB4	PowerVI V 1 OUTPUT OFF	System SEQUENCE DELAY 20000
---	-------------------------------------	------------------------------	-----------------------------------

StaticDigital
MEAS
Current A

System
SAVE AMPS
A Chlp_Leakage_Off

StaticDigital
MEASURE I LIMIT
20 u

StaticDigital
CURRENT MEAS MAX
20 u

PRE MEAS

PowerVI V 1 OUTPUT ON	StaticDigital MEASURE PIN None	StaticDigital MEASURE V FORCE 0	StaticDigital MEASURE MODE Imeas
-----------------------------	--------------------------------------	---------------------------------------	--

RC NOTE

Compile
Run
Repeat



Pulsed DC Measurements

The screenshot shows the 'GSM Pulse' software interface. The menu bar includes File, Edit, Test Plan, Tester, Limits, Options, Help, and Debug. The left sidebar lists 'Test Plan Settings' (Global Defaults, Disconnect Settings, Connect Sequence) and 'Test Section: GSM Pulse Tests; Pulse DC' (Conditional Statement, Section Defaults, **Test: Pulsed DC Current**, Test: Measure RF power in 20 GSM pulses and average, Test: Average Power During GSM Pulse). On the right, there are 'Compile', 'Run', and 'Repeat' buttons.

The main workspace is divided into 'PRE MEAS' and 'POST MEAS' sections. The 'PRE MEAS' section contains two boxes: 'PowerVI' with 'POWER V 1' set to 3, and 'System' with 'SEQUENCE DELAY' set to 200. The 'POST MEAS' section contains a 'PowerVI' box with 'POWER V 1' set to 0.

Below these are two larger configuration boxes. The left one is for 'PowerVI MEAS' with 'Current' set to 'A', 'CURRENT MEAS MAX' set to 1, and 'IMEASURE' set to 'V1'. The right one is for 'System SAVE AMPS' with 'Current after 200 uSec' set to 'A'. A line connects the 'Current' parameter in the PowerVI MEAS box to the 'Current after 200 uSec' parameter in the System SAVE AMPS box. Below the System SAVE AMPS box is a 'System AVERAGES' box with the value 1.

ROOS

NOTE



Pulsed RF Measurements

The screenshot shows the 'GSM Pulse' software interface. The menu bar includes File, Edit, Test Plan, Tester, Limits, Options, Help, and Debug. The left sidebar lists 'Test Plan Settings' (Global Defaults, Disconnect Settings, Connect Sequence) and 'Test Section: GSM Pulse Tests; Pulse DC' (Conditional Statement, Section Defaults, Test: Pulsed DC Current, Test: Measure RF power in 20 GSM pulses and average, Test: Average Power During GSM Pulse). The right sidebar has buttons for Compile, Run, and Repeat. The main workspace contains several measurement blocks:

- System AVERAGES**: Value 8
- System REPEAT**: Value 20
- PRE MEAS**:
 - PowerVI POWER V 1**: Value 3
 - System SEQUENCE DELAY**: Value 25
- POST MEAS**:
 - DutControl VCC 5**: Value 0
 - System SEQUENCE DELAY**: Value 25
 - PowerVI POWER V 1**: Value 0
 - System SEQUENCE DELAY**: Value 1200
- Receiver MEAS**: Value Power
- System LOCAL VAR SAVE**: Value Power during GSM Pulse

A line connects the 'Power' block in the Receiver MEAS section to the 'Power during GSM Pulse' block in the System LOCAL VAR SAVE section.

RO NOTE



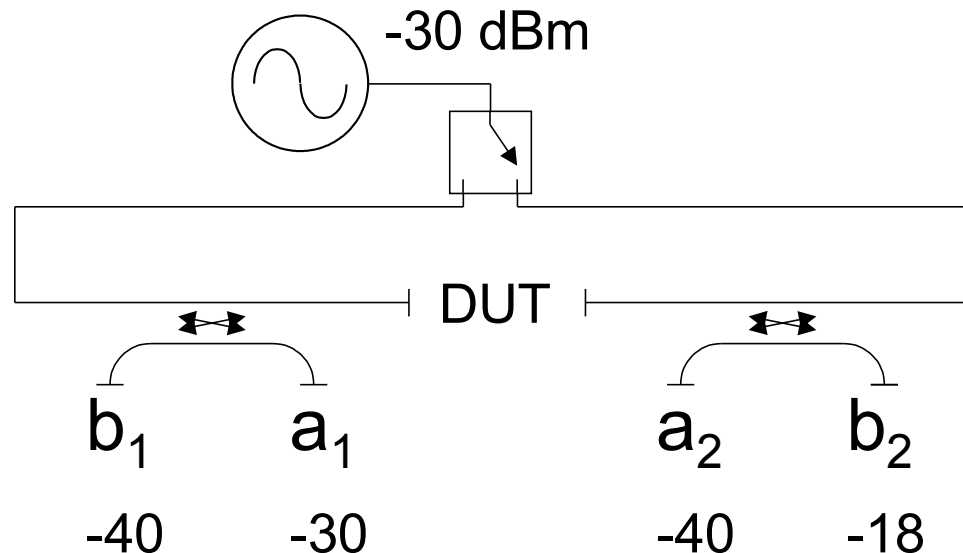
High Dynamic Range Devices

- Wave variation > 30 dB (approx.)
- Waves are a1, a2, b1, b2



Typical Device; LNA

- S21 12 dB
- S11 10 dB
- S12 15 dB
- S22 10 dB

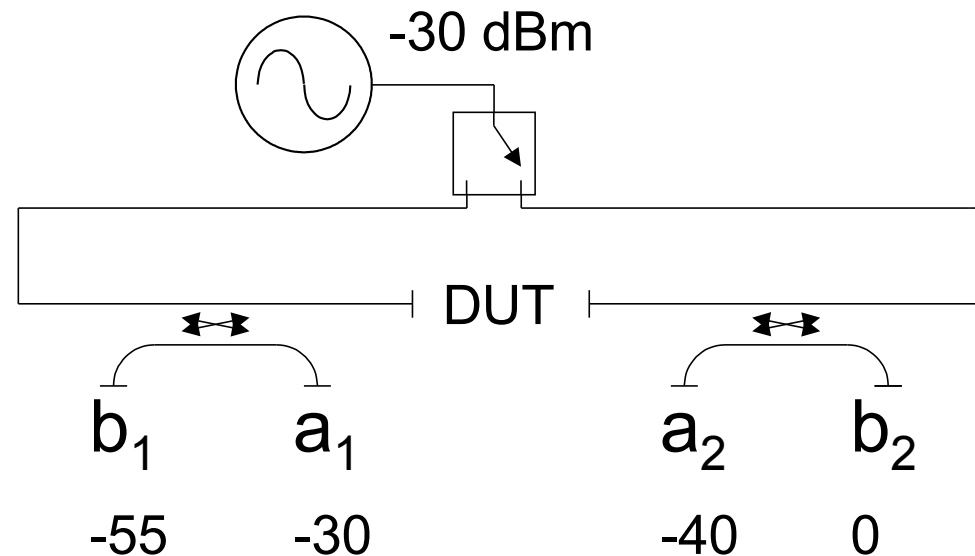


Total Variation 22 dB



High Dynamic Range Device; PA

- S21 30 dB
- S11 10 dB
- S12 25 dB
- S22 10 dB



Total Variation 55 dB



Example HD Devices

- Multi-stage amplifier
- PA
- Limiter
- Filter
- Log Amplifier
- GPS Amplifier



Tester Methods; VNA

- Measures all four waves
- Same Conditions
 - IF Gain
 - Receive Attenuation
- All waves are used to calculate each S-parameter
- Low dynamic range parameters will be influenced by non-optimized ones



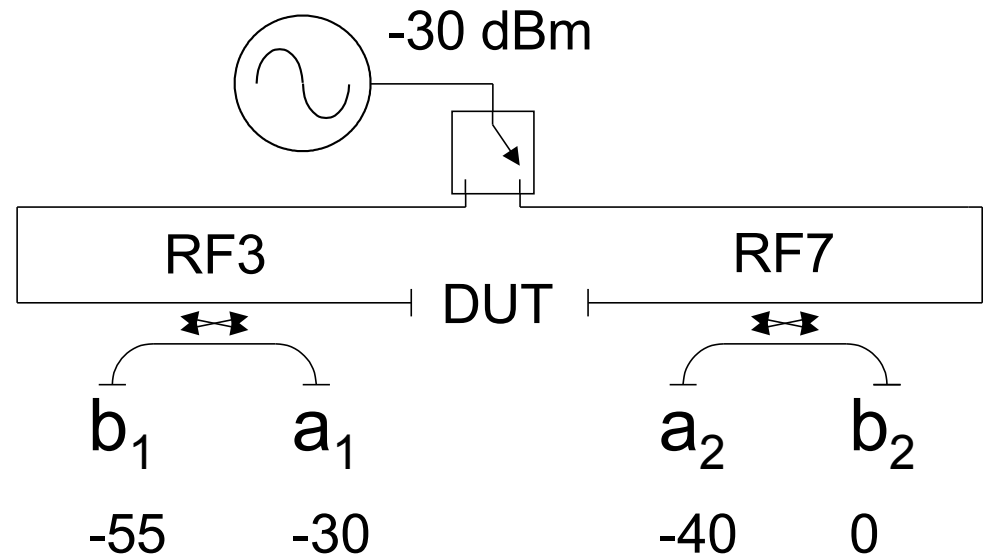
HDD Strategy

- Group according to power variation
- Separate S21 from S12
- Reduce to relevant waves; i.e. S11 only
 - Valid for high dynamic range device
 - If S12 is small; output will not influence input



High Dynamic Range Device; PA

- S21 30 dB
- S11 10 dB
- S12 25 dB
- S22 10 dB

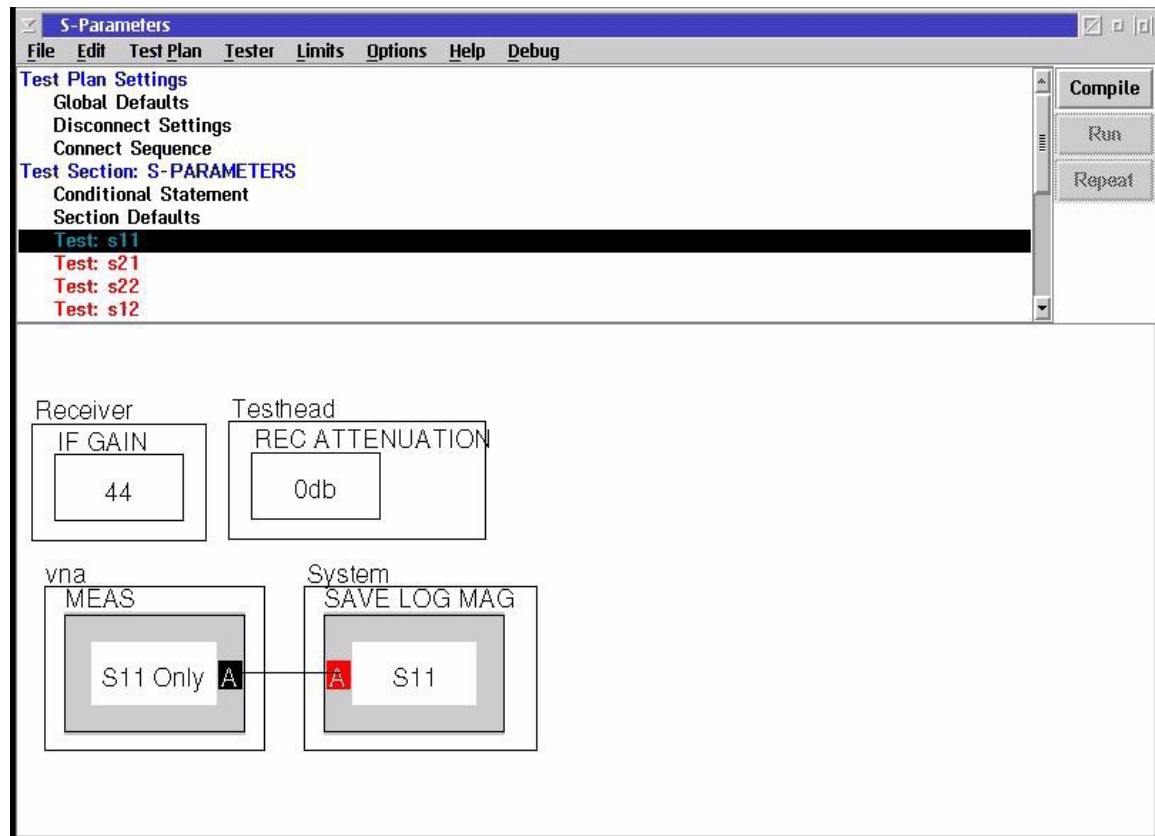


Total Variation 55 dB



S11

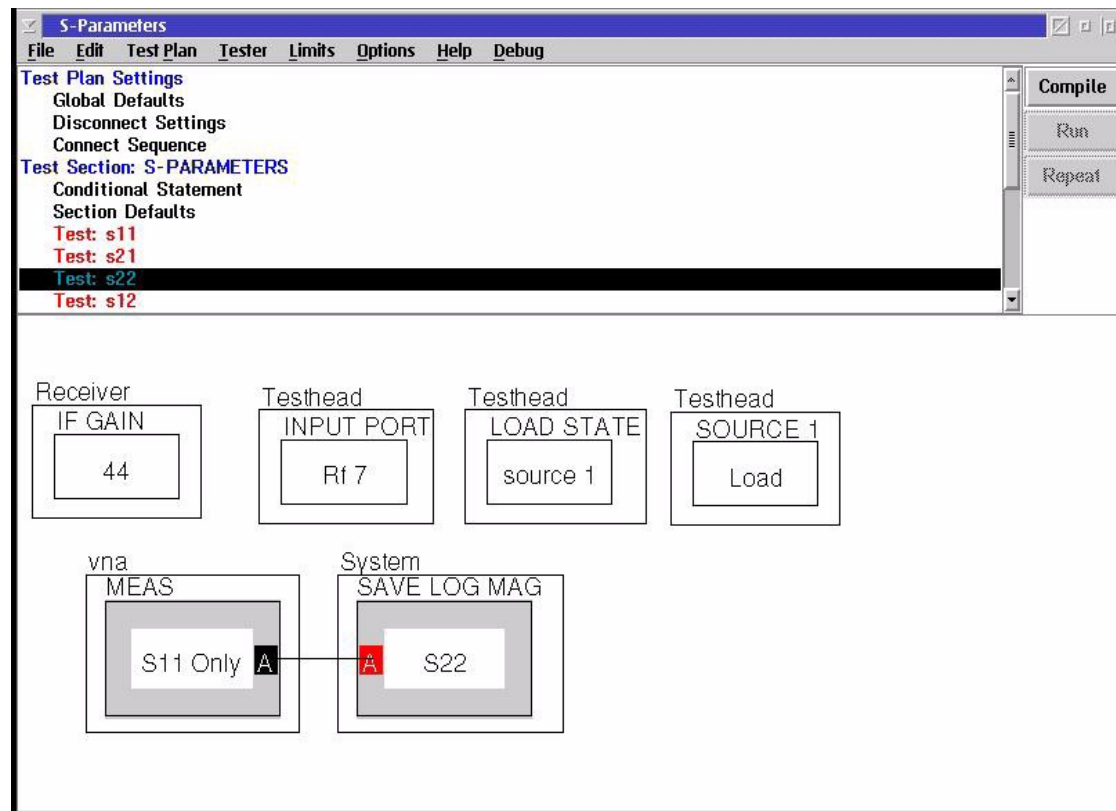
- S11 Only





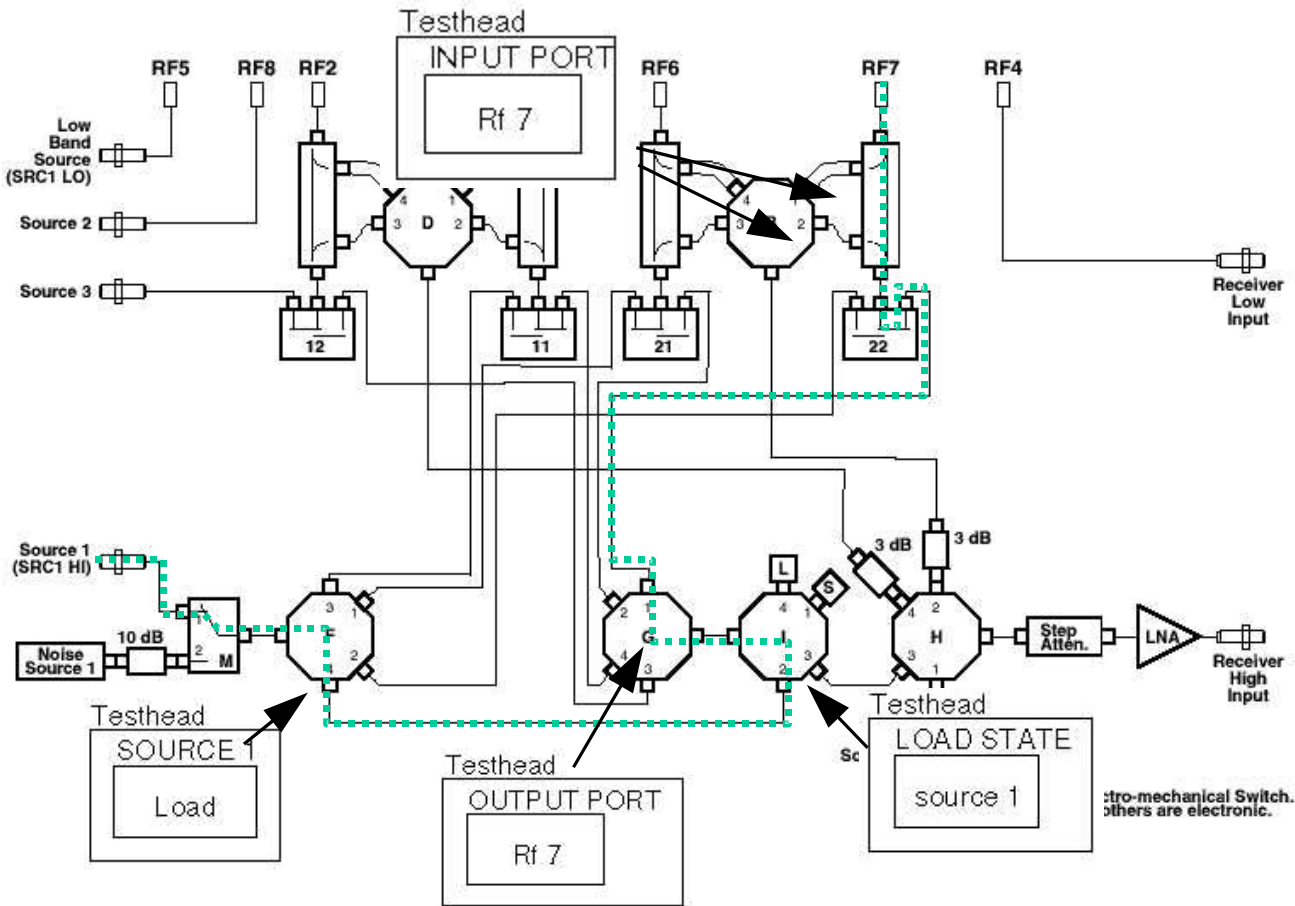
S22

- Back Door





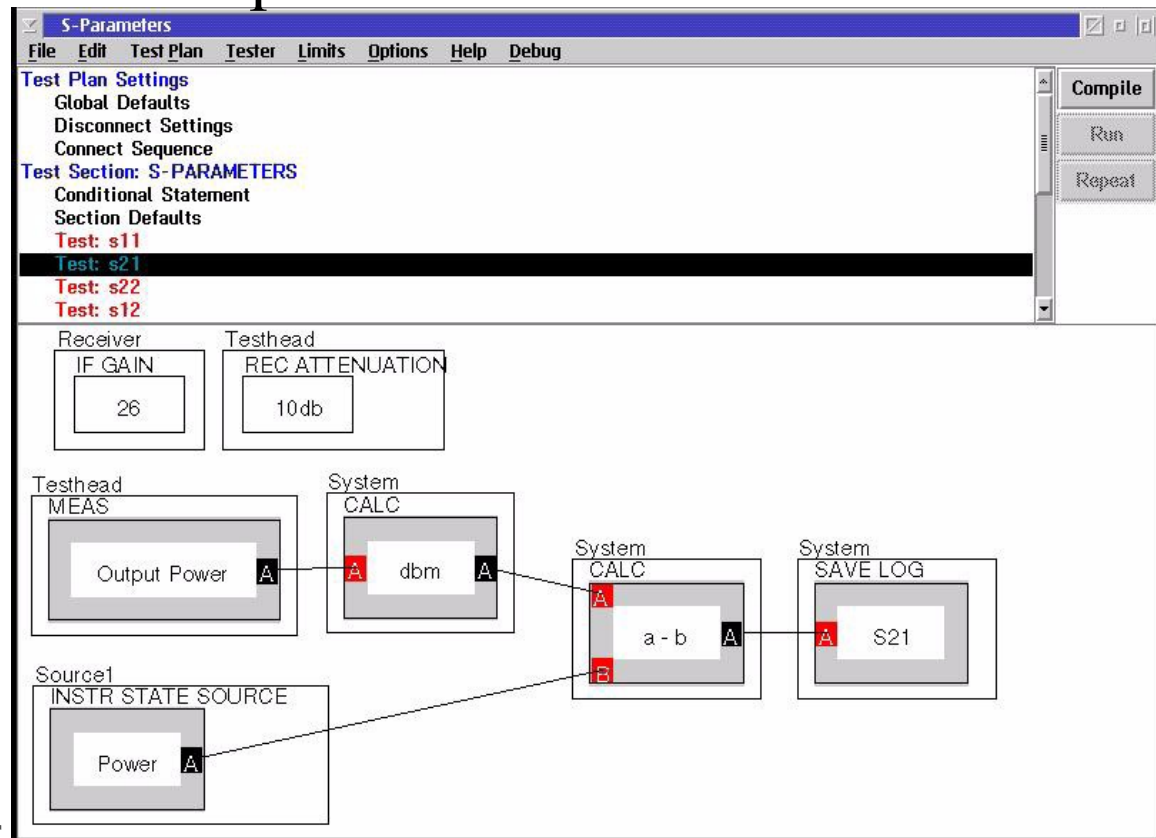
Back Door Path





S21

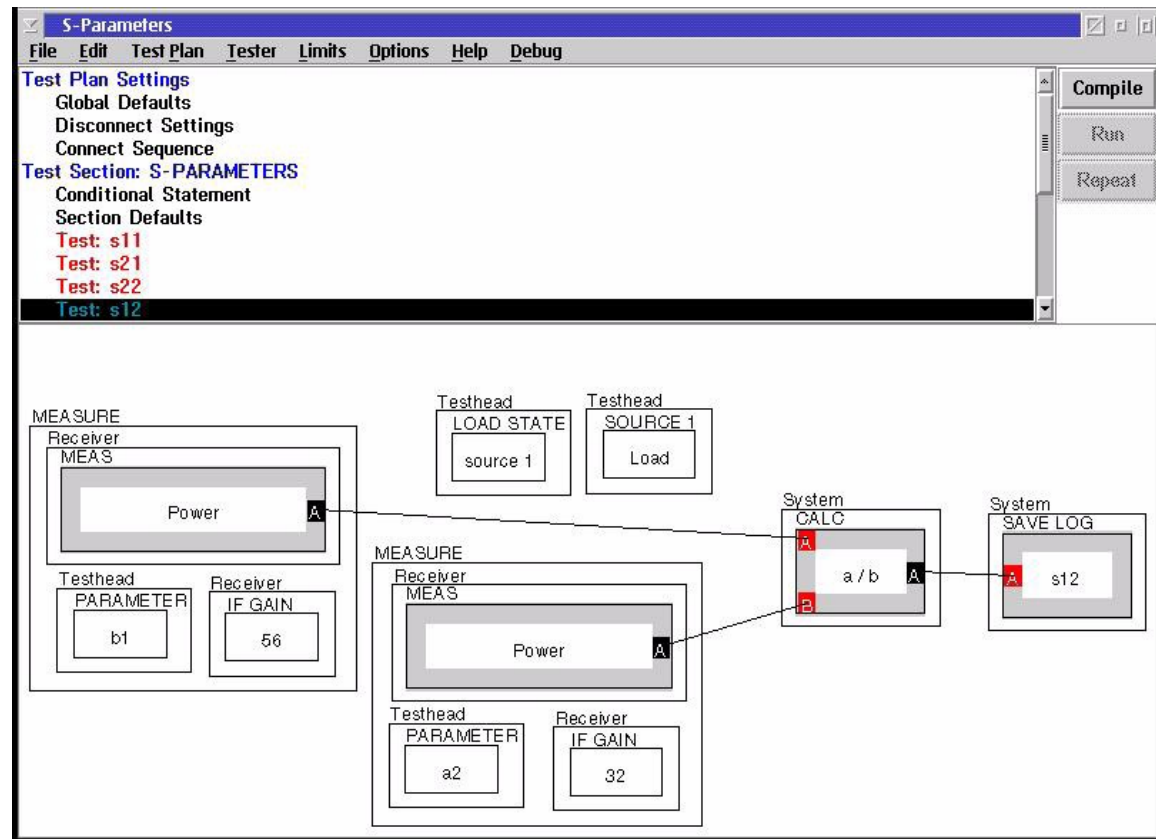
- Only Meas Pout
- Vector Correct for output match





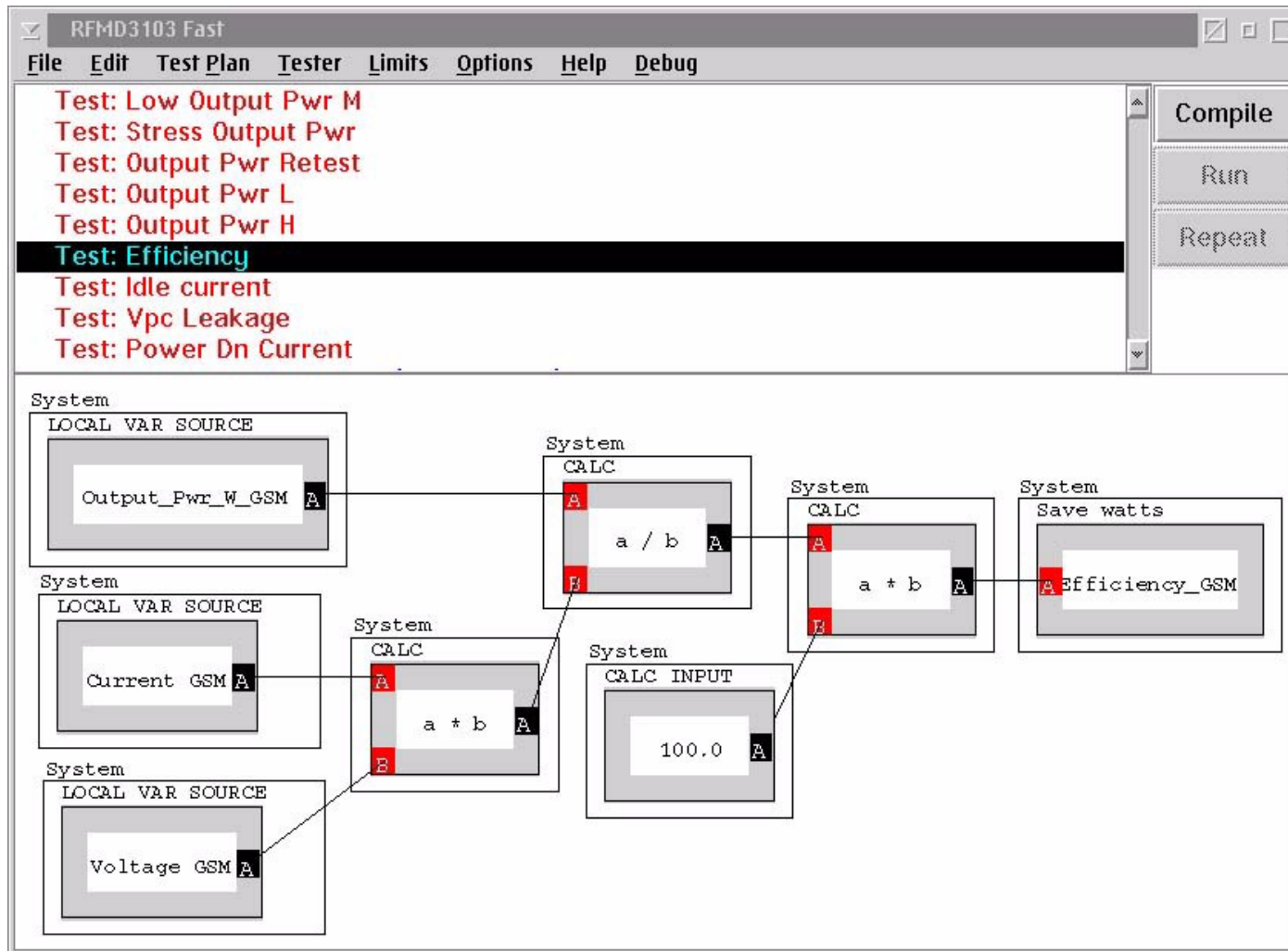
S12

- b1, a2
- back door





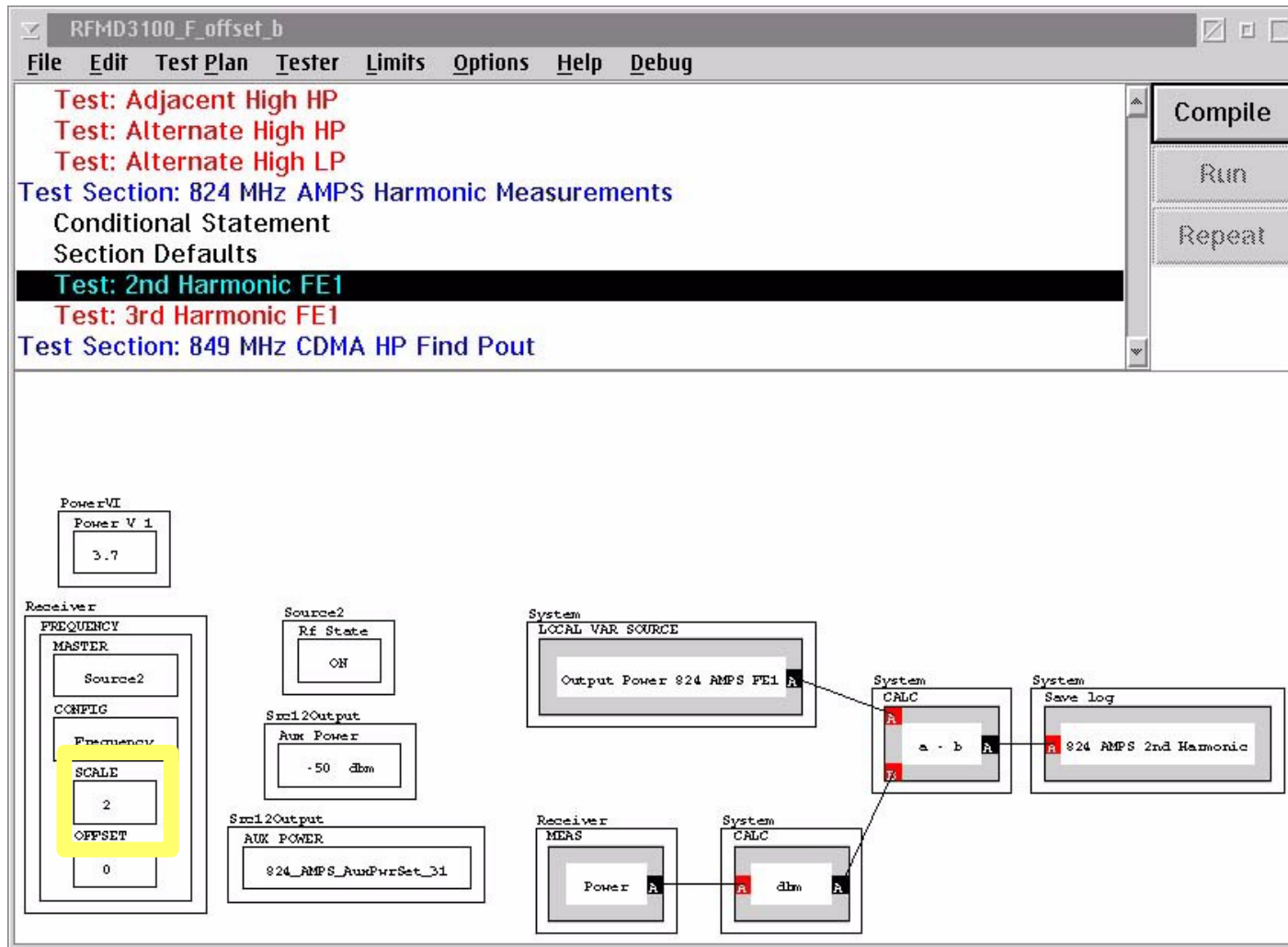
PAE: Power Added Efficiency



ROOS INSTRUMENTS



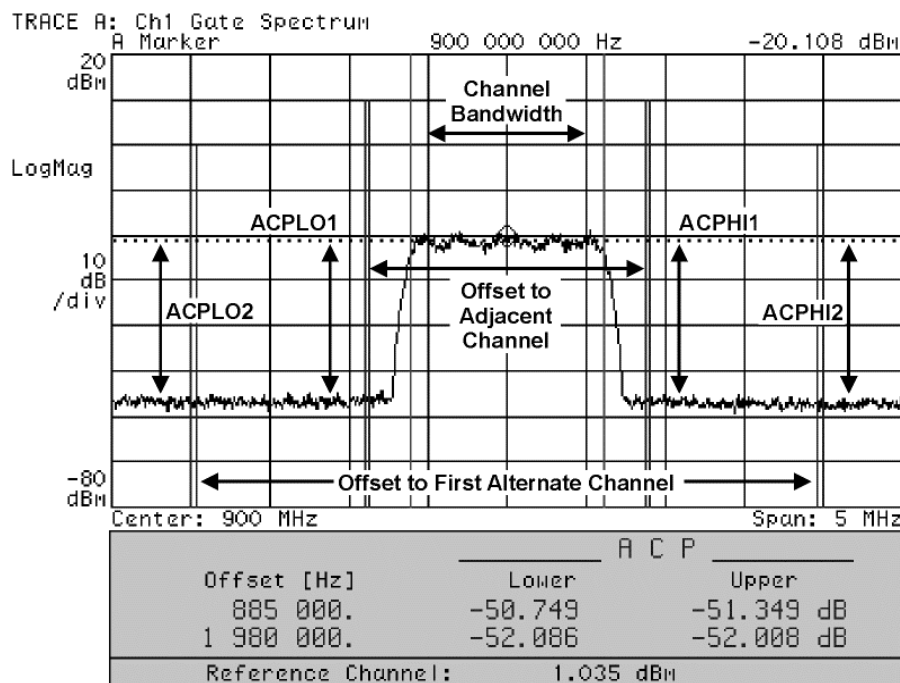
Measure Second Harmonic





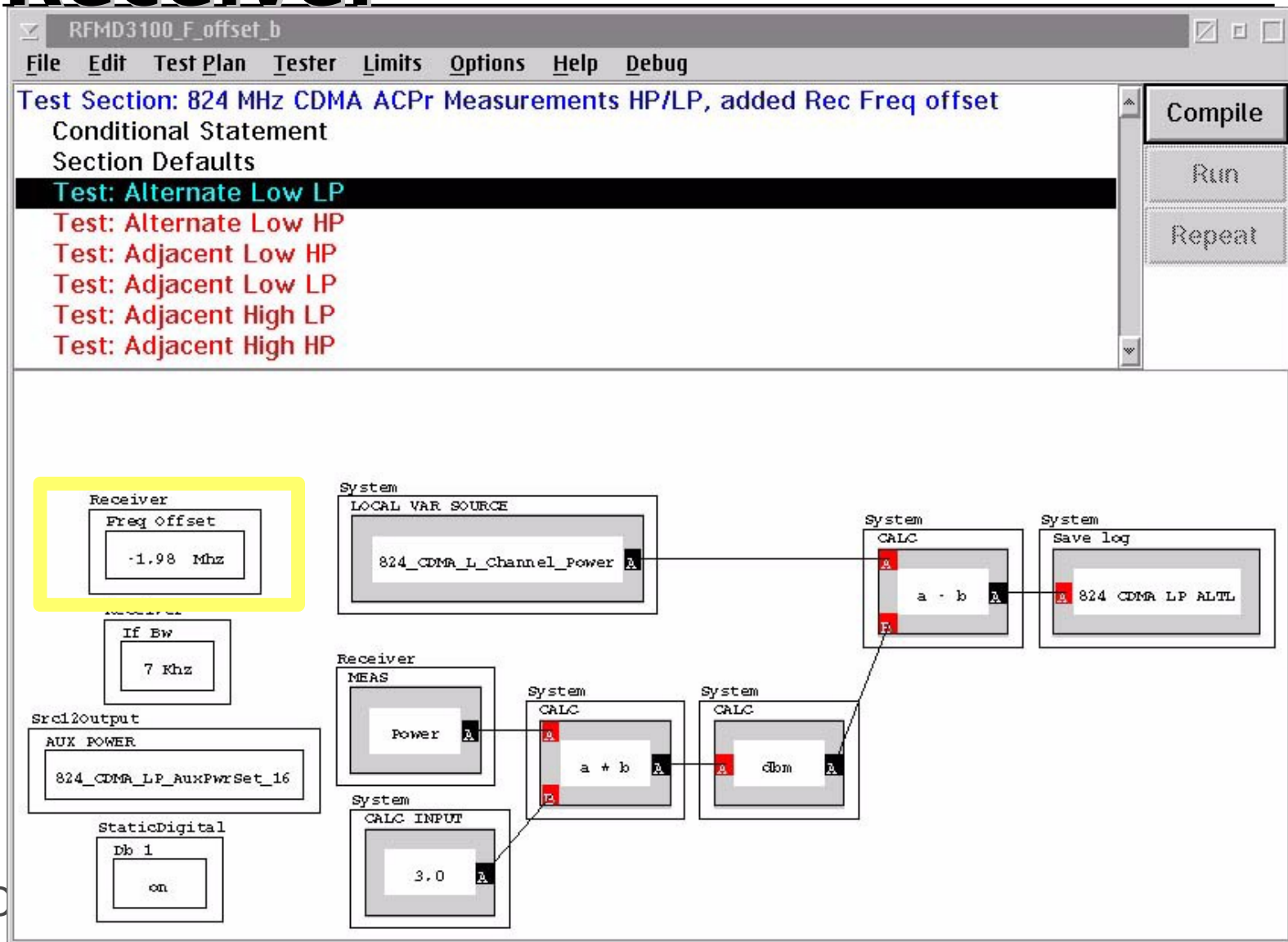
ACPR, ACLR

- "Multi-Tone IP3"
- Must Use RMS
- Power in Specified Bandwidth
- Every Standard is Different





Measure ACPR using Receiver



RC



Sweep Power to Find Gain Slope Use Lock Step to Control Receiver Attenuation

File Edit Test Plan Tester Limits Options Help Debug

Test Section: Gain Slope GSM (Unoptimized)
Conditional Statement
Section Defaults
Test: Gain Slope L
Test: Gain Slope H
Test: Calculation Low Power Log
Test: Calculation High Power Log
Test: Calculation High Power Linear

Test Section: GSM Tests (Unoptimized)

LOCK STEP CONFIGS

PowerVI Power V 3 1.08	Testhead Rec Attenuation 20db
PowerVI Power V 3 1.09	Testhead Rec Attenuation 20db
PowerVI Power V 3 1.1	Testhead Rec Attenuation 30db
PowerVI Power V 3 1.12	Testhead Rec Attenuation 30db
PowerVI Power V 3 1.14	Testhead Rec Attenuation 30db

If Gain
44

PRE MEAS

PowerVI Power V 3 A	System Sequence Delay 0
---------------------------	-------------------------------

POST MEAS

PowerVI Power V 3 0

PowerVI
INSTR STATE SOURCE
PowerV3

Receiver
MEAS
Power

System
CALC
dbm

System
CALC
voltage

System
CALC INPUT
1.414

System
LOCAL VAR SAVE
V_Gn_Slp_GSM

System
LOCAL VAR SAVE
F_dB_Gn_Slp_GSM

System
CALC
a * b

System
LOCAL VAR SAVE
F_VGn_Slp_GSM



PA Test Plan

- Examine Example PA Test Plan

PA_Lab_RevA

File Edit Test Plan Tester Limits Options Help Debug

Test Plan Settings

- Global Defaults
- Disconnect Settings
- Connect Sequence
- Test Section: DC Test
 - Conditional Statement
 - Section Defaults
 - Test: Leakage Test
- Test Section: Quiescent Current
 - Conditional Statement
 - Section Defaults
 - Test: Quiescent Current

Compile

Run

Repeat

Receiver

FREQUENCY

MASTER

Aux Source

CONFIG

Frequency

SCALE

1

OFFSET

0

System

Freq Reference

Aux Source

Out Freq Offset

0

Out Freq Scale

1

Testhead

Rf 3

src1-noise

Testhead

Input Port

Rf 3

Aux Source

Frequency

880 Mhz

Power

10 dbm

Testhead

RE 7

receive

Testhead

Output Port

Rf 7

Aux Source

Modulation

CDMA

Testhead

Source 1 Mode

source

Testhead

Source 1

RF 3

System

Averages

16

Receiver

If Gain

40*

Testhead

Parameter

b2

Testhead

Rec Attenuation

30db

Src12Output

Source Output Mode

Aux to src 1

Src12Output

Source 1 Attn

10db

PowerVI

Power V 1

3

Power I 1

1

V 1 Output

OFF

StaticDigital

Voff

0

StaticDigital

Von

3

StaticDigital

Db 1

open

StaticDigital

Db 2

off

PA_Lab_RevA

File Edit Test Plan Tester Limits Options Help Debug

Test Plan Settings
Global Defaults
Disconnect Settings
Connect Sequence
Test Section: DC Test
Conditional Statement
Section Defaults
Test: Leakage Test
Test Section: Quiescent Current
Conditional Statement
Section Defaults
Test: Quiescent Current

Compile
Run
Repeat

Src12Output

Aux Power

-32 dbm

NOTE

PA_Lab_RevA

File Edit Test Plan Tester Limits Options Help Debug

Test Plan Settings

- Global Defaults
- Disconnect Settings
- Connect Sequence**

Test Section: DC Test

- Conditional Statement
- Section Defaults
- Test: Leakage Test**

Test Section: Quiescent Current

- Conditional Statement
- Section Defaults
- Test: Quiescent Current**

Compile

Run

Repeat

NOTE

PA_Lab_RevA

File Edit Test Plan Tester Limits Options Help Debug

Test Plan Settings
Global Defaults
Disconnect Settings
Connect Sequence

Test Section: DC Test
Conditional Statement
Section Defaults

Test: Leakage Test

Test Section: Quiescent Current
Conditional Statement
Section Defaults

Compile
Run
Repeat

StaticDigital
Measure Mode
I meas

StaticDigital
Measure V Force
3

StaticDigital
Measure Pin
DB1

StaticDigital
Current Meas Max
100 u

StaticDigital
Measure I Limit
100 u

StaticDigital
MEAS
Current

System
Save Amps
Leakage Current

PA_Lab_RevA

File Edit Test Plan Tester Limits Options Help Debug

Test Section: Quiescent Current
Conditional Statement
Section Defaults
Test: Quiescent Current

Test Section: CDMA Power Sweep
Conditional Statement
Section Defaults
Test: Sweep Aux Power CDMA
Test: Find Aux Power in for 30dBm out

Test Section: PDC DC and ACP Test
Conditional Statement
Section Defaults

StaticDigital

Db 2

on

Compile

Run

Repeat

PA_Lab_RevA

File Edit Test Plan Tester Limits Options Help Debug

Test Section: Quiescent Current
Conditional Statement
Section Defaults
Test: Quiescent Current
Test Section: CDMA Power Sweep
Conditional Statement
Section Defaults
Test: Sweep Aux Power CDMA
Test: Find Aux Power in for 30dBm out
Test Section: PDC DC and ACP Test
Conditional Statement
Section Defaults

Compile
Run
Repeat

PowerVI

MEAS

Current A

System

Save Ampe

A Quiescent Current

CURRENT MEAS MAX

0.1

IMEASURE

V1

PowerVI

Power I 1

0.1

PA_Lab_RevA

File Edit Test Plan Tester Limits Options Help Debug

Test Section: CDMA Power Sweep
Conditional Statement
Section Defaults
Test: Sweep Aux Power CDMA
Test: Find Aux Power in for 30dBm out

Test Section: PDC DC and ACP Test
Conditional Statement
Section Defaults
Test: Power Current
Test: Pin
Test: Target Power (Test is optional, Pout is should be 8dBm from sweep)
Test: PAF

StaticDigital

Db 2

on

Compile

Run

Repeat

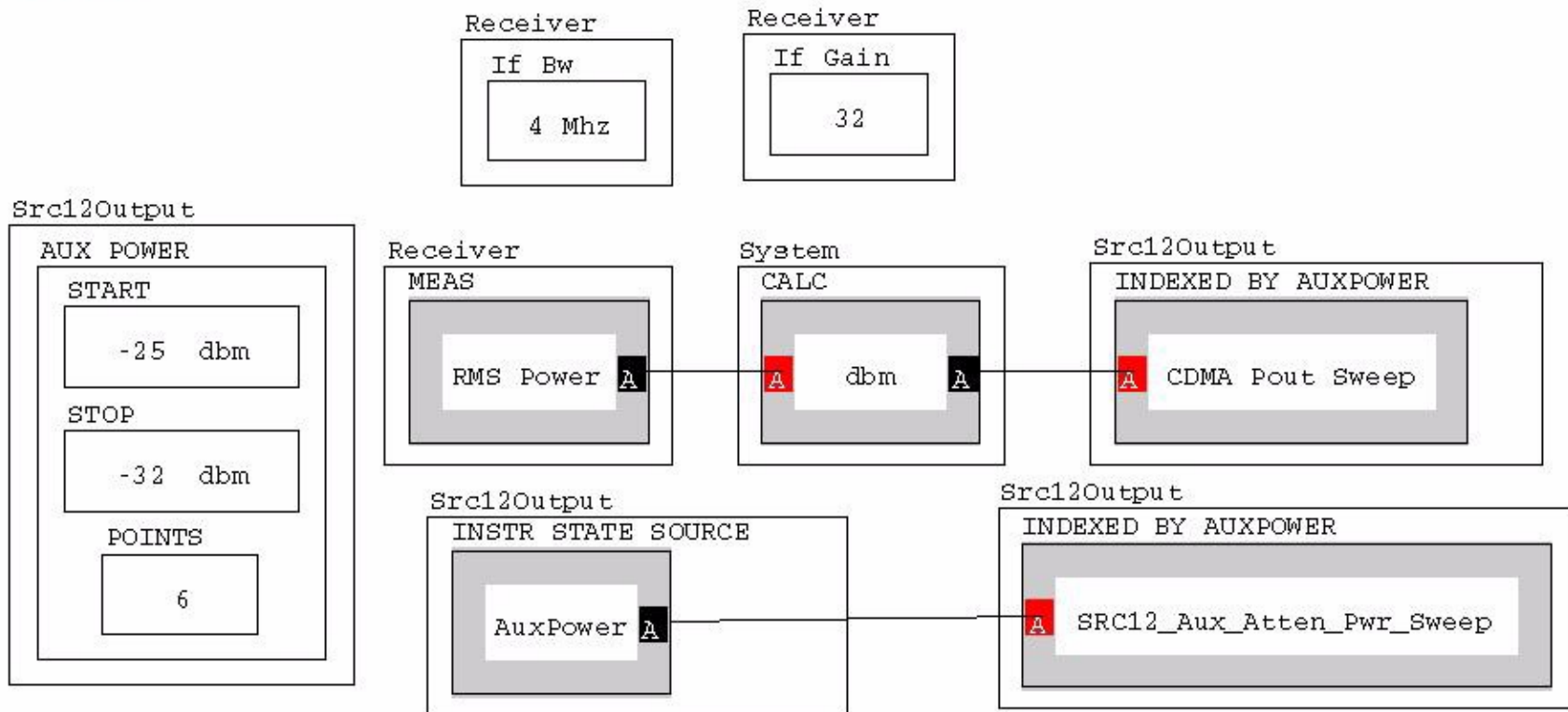
PA_Lab_RevA

File Edit Test Plan Tester Limits Options Help Debug

Test Section: CDMA Power Sweep
 Conditional Statement
 Section Defaults
Test: Sweep Aux Power CDMA
 Test: Find Aux Power in for 30dBm out

Test Section: PDC DC and ACP Test
 Conditional Statement
 Section Defaults
 Test: Power Current
 Test: Pin
 Test: Target Power (Test is optional, Pout is should be 8dBm from sweep)
 Test: PAF

Compile
 Run
 Repeat



PA_Lab_RevA

File Edit Test Plan Tester Limits Options Help Debug

Test Section: PDC DC and ACP Test

- Conditional Statement
- Section Defaults
- Test: Power Current**
- Test: Pin
- Test: Target Power (Test is optional, Pout is should be 8dBm from sweep)
- Test: PAE
- Test: ACPr 1 Hi
- Test: ACPr 1 Lo
- Test: ACPr 2 Hi
- Test: ACPr 2 Lo

Compile

Run

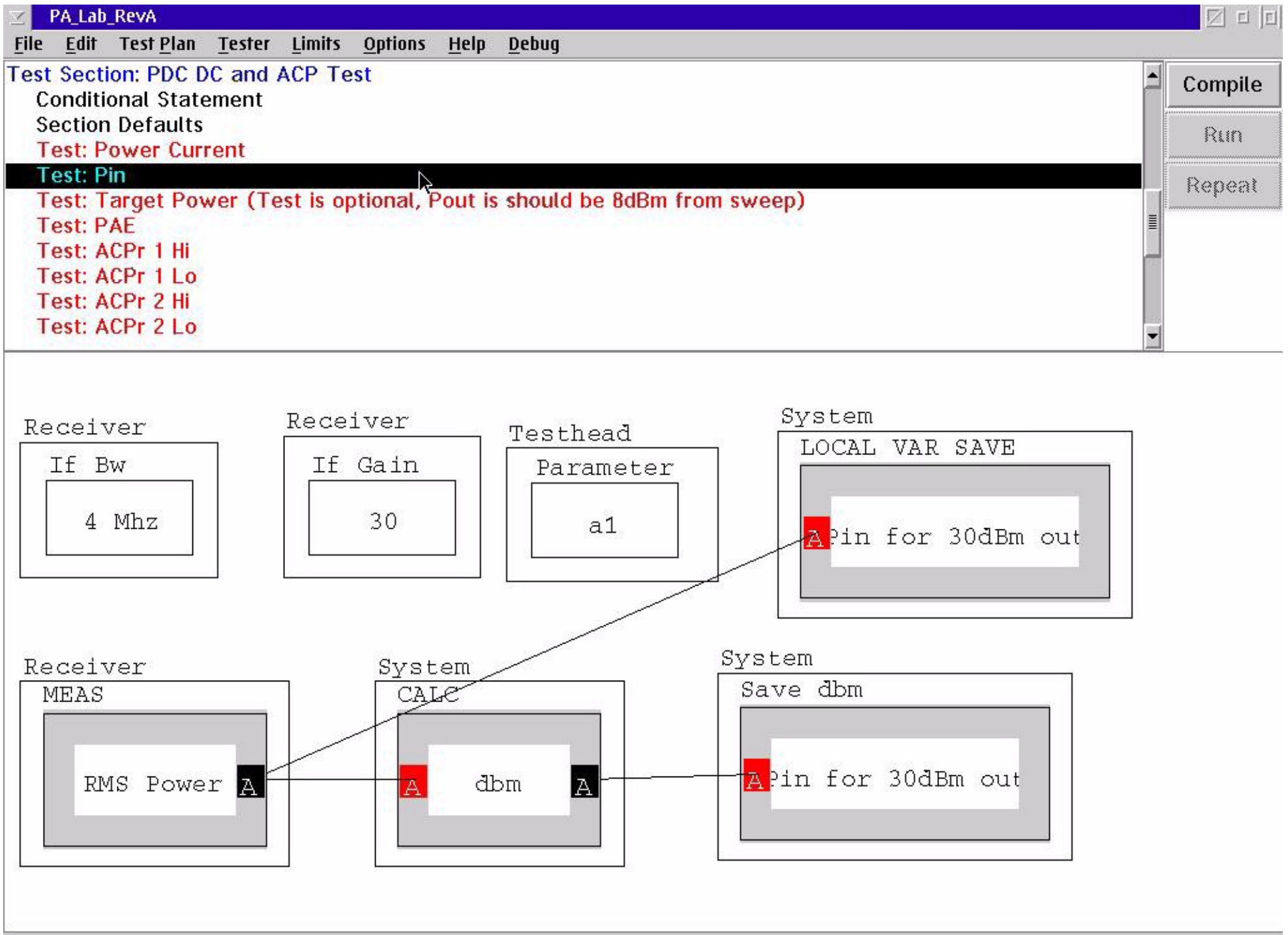
Repeat

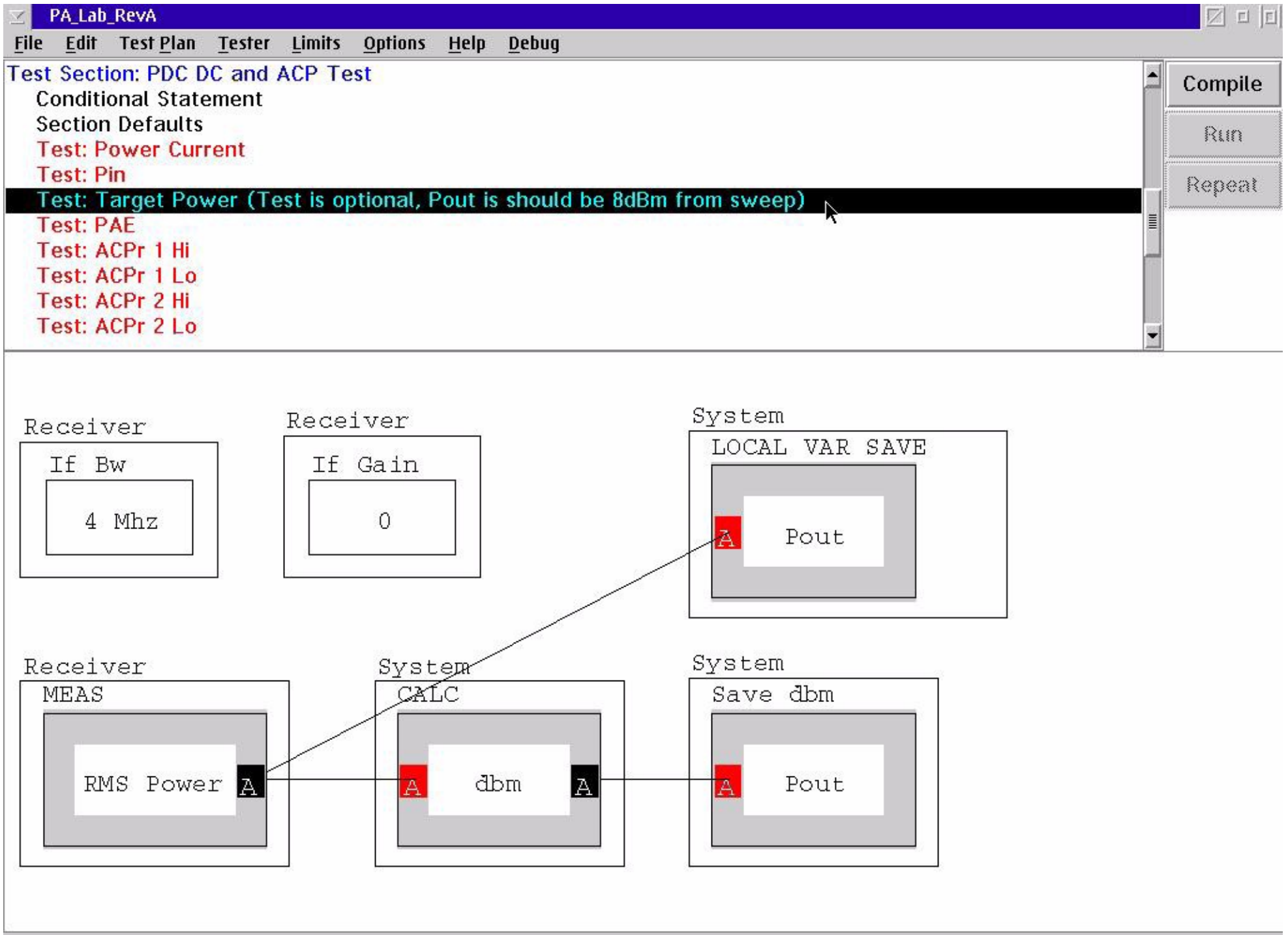
The diagram illustrates the test setup for Power Current and Power Voltage. It consists of several interconnected blocks:

- PowerVI MEAS**: Contains a **Current** block with a red 'A' icon. It is connected to the **Power Current** block in the **System Save Amps** and **System LOCAL VAR SAVE** blocks.
- PowerVI INSTR STATE SOURCE**: Contains a **PowerVI** block with a red 'A' icon. It is connected to the **Power Voltage** block in the **System LOCAL VAR SAVE** block.
- System Save Amps**: Contains a **Power Current** block with a red 'A' icon.
- System LOCAL VAR SAVE**: Contains a **Power Current** block with a red 'A' icon and a **Power Voltage** block with a red 'A' icon.
- PowerVI Power I 1**: A block containing a **1** value.

Additional parameters in the PowerVI MEAS block include:

- CURRENT MEAS MAX: 1
- IMEASURE: VI





PA_Lab_RevA

File Edit Test Plan Tester Limits Options Help Debug

Test Section: PDC DC and ACP Test

Conditional Statement

Section Defaults

Test: Power Current

Test: Pin

Test: Target Power (Test is optional, Pout is should be 8dBm from sweep)

Test: PAE

Test: ACPr 1 Hi

Test: ACPr 1 Lo

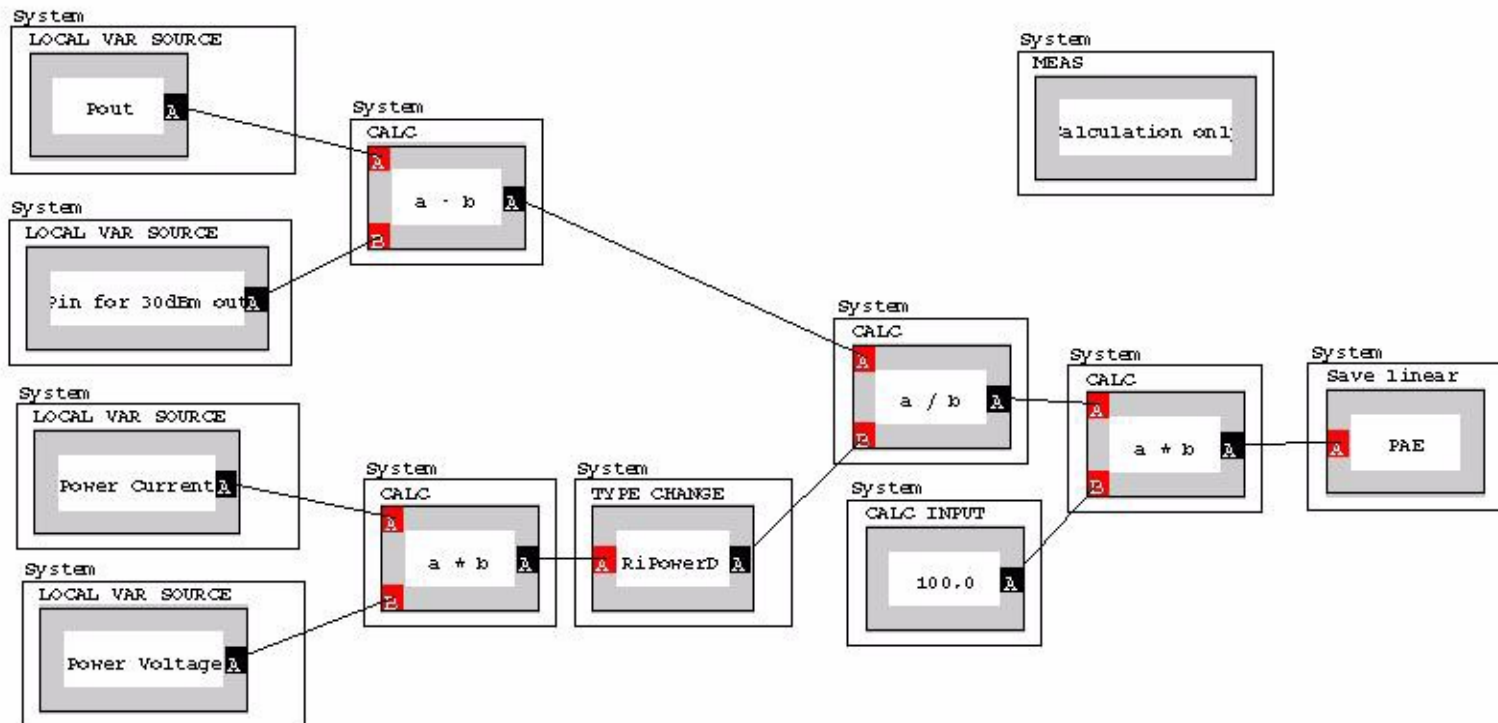
Test: ACPr 2 Hi

Test: ACPr 2 Lo

Compile

Run

Repeat



PA_Lab_RevA

File Edit Test Plan Tester Limits Options Help Debug

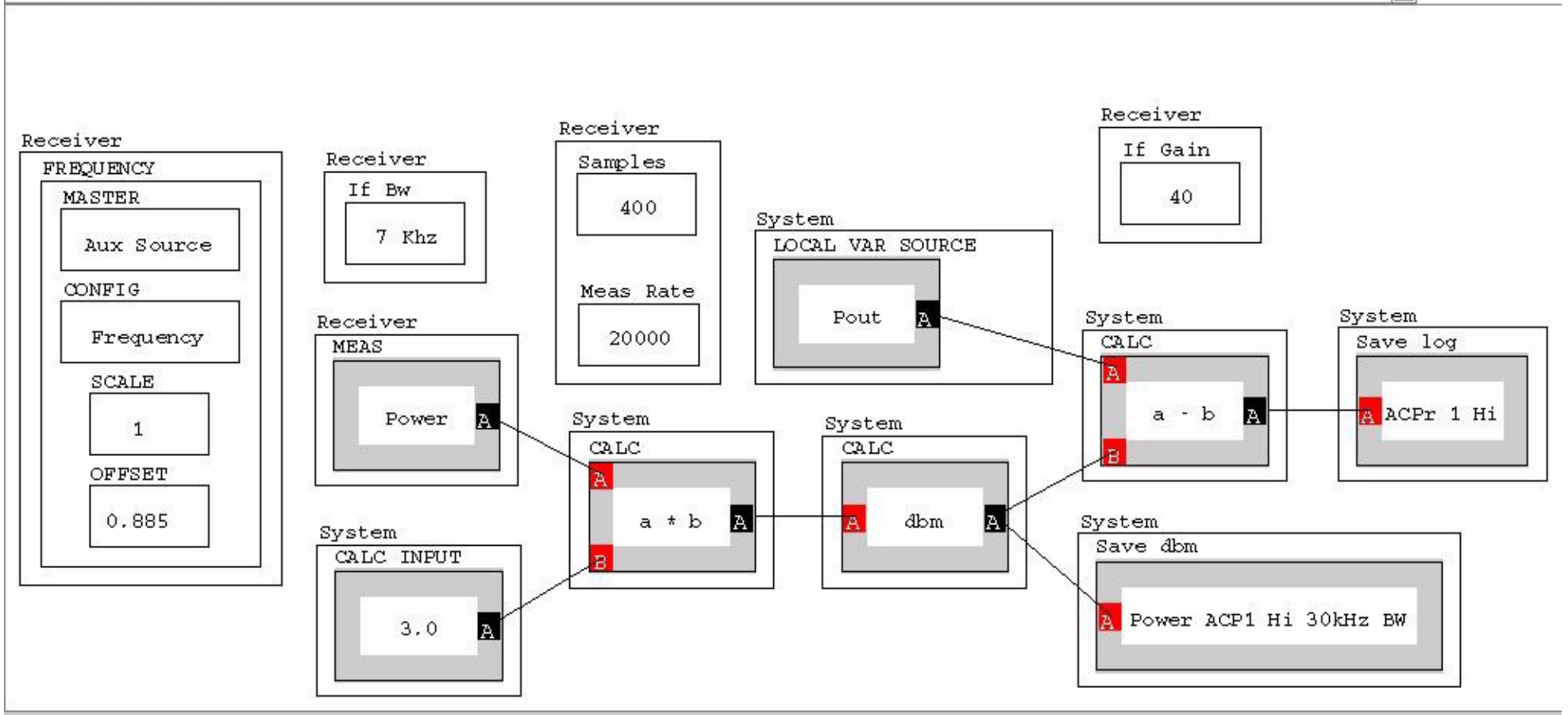
Test Section: PDC DC and ACP Test

- Conditional Statement
- Section Defaults
- Test: Power Current
- Test: Pin
- Test: Target Power (Test is optional, Pout is should be 8dBm from sweep)
- Test: PAE
- Test: ACPr 1 Hi**
- Test: ACPr 1 Lo
- Test: ACPr 2 Hi
- Test: ACPr 2 Lo

Compile

Run

Repeat



PA_Lab_RevA

File Edit Test Plan Tester Limits Options Help Debug

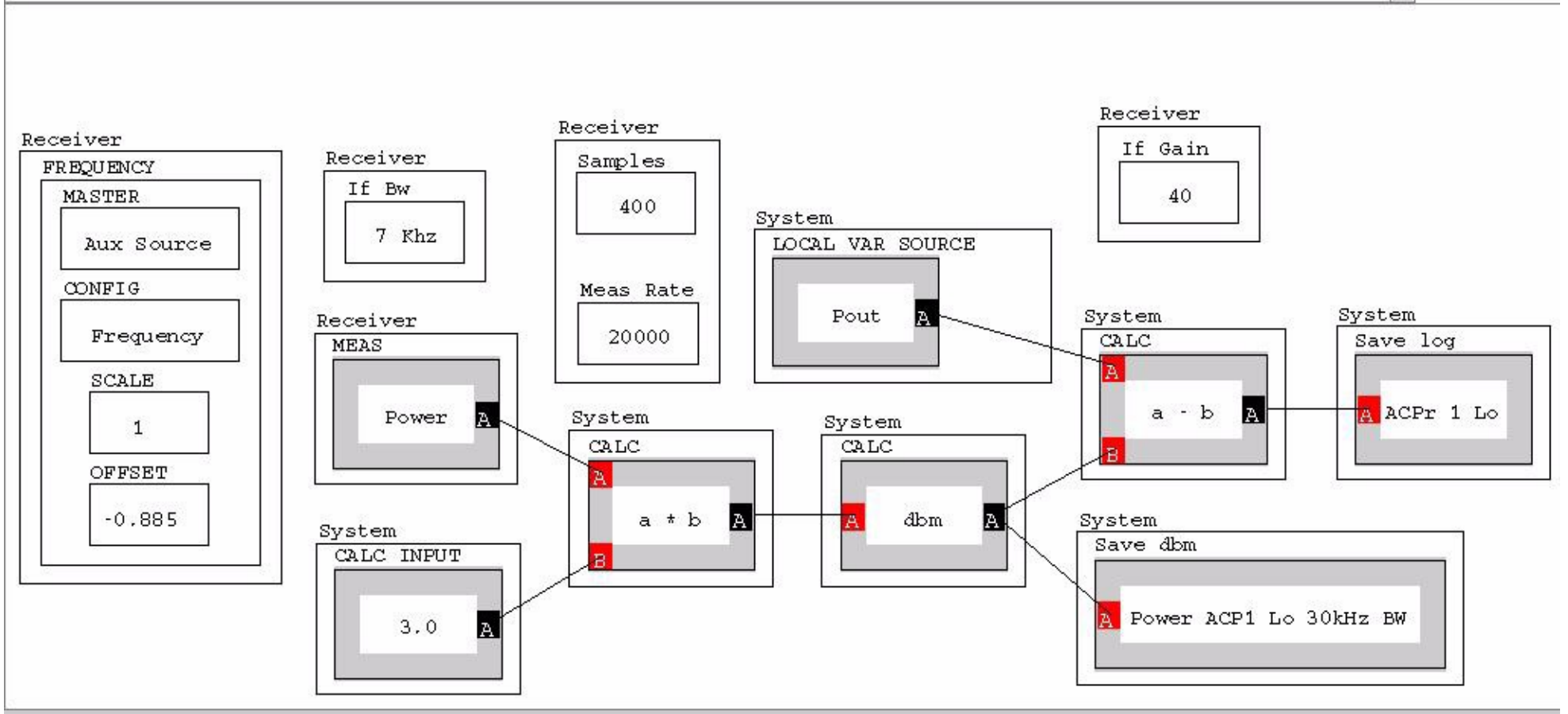
Test Section: PDC DC and ACP Test

- Conditional Statement
- Section Defaults
- Test: Power Current
- Test: Pin
- Test: Target Power (Test is optional, Pout is should be 8dBm from sweep)
- Test: PAE
- Test: ACPr 1 Hi
- Test: ACPr 1 Lo**
- Test: ACPr 2 Hi
- Test: ACPr 2 Lo

Compile

Run

Repeat



PA_Lab_RevA

File Edit Test Plan Tester Limits Options Help Debug

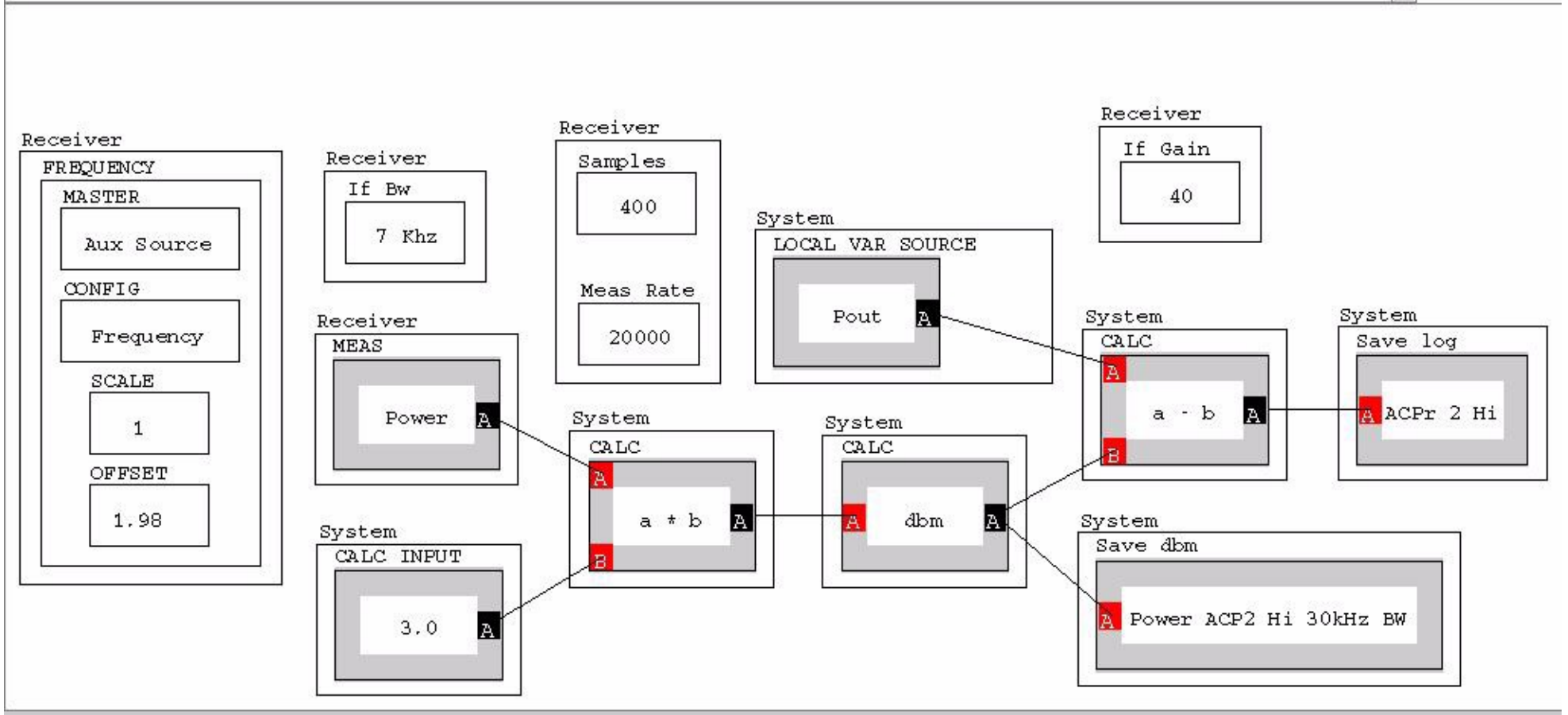
Test Section: PDC DC and ACP Test

- Conditional Statement
- Section Defaults
- Test: Power Current
- Test: Pin
- Test: Target Power (Test is optional, Pout is should be 8dBm from sweep)
- Test: PAE
- Test: ACPr 1 Hi
- Test: ACPr 1 Lo
- Test: ACPr 2 Hi**
- Test: ACPr 2 Lo

Compile

Run

Repeat



PA_Lab_RevA

File Edit Test Plan Tester Limits Options Help Debug

Test Section: PDC DC and ACP Test

Conditional Statement

Section Defaults

Test: Power Current

Test: Pin

Test: Target Power (Test is optional, Pout is should be 8dBm from sweep)

Test: PAE

Test: ACPr 1 Hi

Test: ACPr 1 Lo

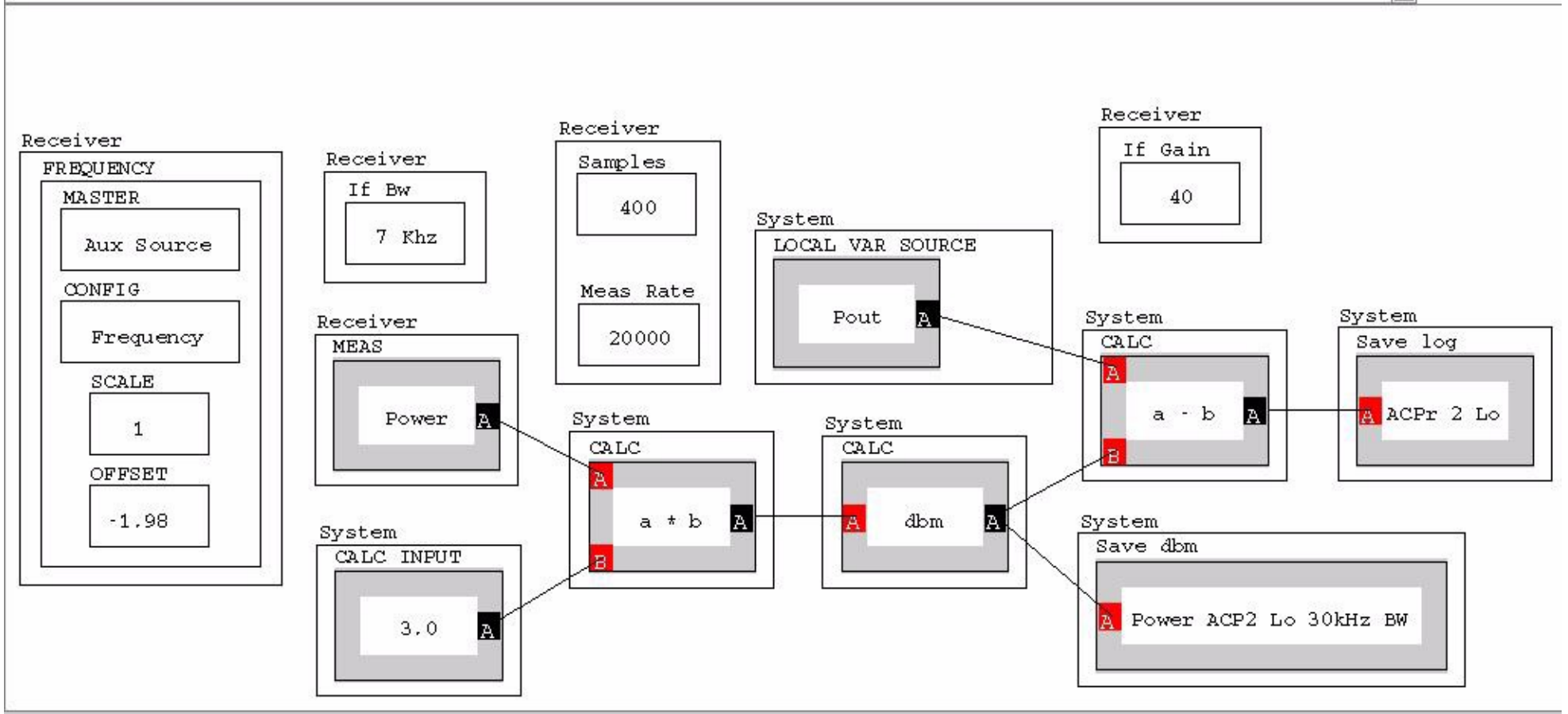
Test: ACPr 2 Hi

Test: ACPr 2 Lo

Compile

Run

Repeat





Example Applications - Lab E

- Get into Groups of Three
- Each will take turns performing the lab
- One drives, one reads, one uses pointer



PA Test Plan Lab: ACPR Test

- Use Aux Source
- Measure Leakage
- Search and Fix Pout
- Measure CDMA ACPR
 - 1.23 MHz Channel
 - 885 kHz, 1980 kHz Offset; 30 kHz BW



PA Test Plan Lab: NADC ACPR

- Create NADC Measurement
 - 25 kHz Ch.; 30 kHz Offset 25 kHz BW
- Channel is Flat
- Significant Power exists outside the channel
- Pout Does Not Equal Channel Power